DEC STD 030-4
MODULE MANUFACTURING STANDARD— PRINTED-WIRING BOARD DESIGN REQUIREMENTS

DOCUMENT IDENTIFIER: A-DS-EL00030-04-0 Rev E, 17-June-1991

ABSTRACT: This section of DEC STD 030 provides the design and design selection requirements for all printed-wiring boards.

APPLICABILITY: This standard is mandatory for designs to be compatible with the standard volume manufacturing process. Site Producibility Engineers are available to provide additional information on specific areas not covered in this standard.

STATUS: APPROVED 17-June-1991; use VTX SMC for current status.

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APPROVAL: This document has been reviewed and recommended for approval by the DEC STD 030 Advisory Committee and the General Review Group for its category.

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1 INTRODUCTION

This section of DEC STD 030 provides the design and design selection rules for all printed-wiring boards. Certain rules provide options designated as preferred, acceptable, or risk, which are defined as follows:

a. Preferred

1. Qualified PWB supplier process capability/manufacturing capacity exceed needs
2. No PWB supplier process development required
3. No qualification required
4. Lowest PWB cost approach
5. Shortest time-to-market approach

b. Acceptable

1. Qualified PWB supplier process capability/manufacturing capacity approximate needs
2. Minimal PWB supplier process development may be required
3. Minimum qualification may be required
4. Higher PWB cost than preferred approach
5. Longer time-to-market than preferred approach

c. Risk

1. Qualified PWB supplier process capability/manufacturing capacity may be deficient
2. Significant PWB supplier process development may be required
3. Formal qualification may be required
4. Highest PWB cost approach
5. Longest time-to-market approach
6. Waiver may be required. Refer to DEC STD 030-1, Rule 1030 and DEC STD 030-1, Exhibit 6.

d. Unacceptable

1. Attributes designated as unacceptable are not allowed under any circumstance.
2. Waiver required. Refer to DEC STD 030-1, Rule 1030 and DEC STD 030-1, Exhibit 6.

For information regarding 50-class qualified PWB suppliers, contact Gerald Gagnon, DTN 226-2037, BOARDS::GAGNON.

2 DESIGN SELECTION RULES

This heading defines standard circuit technology features to aid design sites in design selection.

RULE 4000: STANDARD CIRCUIT TECHNOLOGY

In past revisions of this standard, the manufacturability limits for the quantity and variety of circuit features were defined and published under this rule as Standard Circuit Technology Definitions. The basis for these definitions was the Gerber Photoplotter aperture wheel restrictions. These restrictions are no longer valid due to the extensive use of laser photoplotting within the PWB industry. However, because these definitions have been used in past designs that are still highly manufacturable today, these definitions have been retained and placed in Appendix A. Refer to Appendix A, Exhibit 26, Exhibit 27, and Exhibit 28, respectively, for the standard circuit technology definitions, associated inner layer clearance pad table, and the spacing reference guide.

Design sites may choose circuit technology features defined in the Appendix A exhibits or select more manufacturable designs that meet the requirements stated in the following subheads.

RULE 4010: SIGNAL PAD AND INNER LAYER CLEARANCE PAD DIAMETER SELECTION

The nominal values of standard finished hole sizes (FHS) required by stage 1 assembly and the rules for determining unique finished hole size nominal values are given in DEC STD 030-5, Exhibit 4 and DEC STD 030-5, Exhibit 6.

It is recommended that a minimum number of different finished hole sizes be selected to reduce setup and drilling times in board manufacturing.

Exhibit 1 gives the nominal diameters of signal pads and inner layer clearance pads as determined from the standard nominal finished hole sizes.

RULE 4011: NONPLATED-THROUGH HOLES

Design requirements for nonplated-through holes (NPTHs) are as follows.

a. NPTHs shall have no pads on outer layers.

b. NPTHs shall have inner layer clearance pads on inner layers. Refer to Exhibit 1 for clearance pad diameters if there are no functional characteristics that warrant increased clearances.

c. NPTHs shall have nominal diameters less than or equal to 0.250 inch.

d. When necessary, nominal diameters greater than 0.250 inch shall be positionally dimensioned and routed to size.

RULE 4012: ASPECT RATIOS

The aspect ratio of board thickness to finished hole size shall be as follows.

a. Preferred - $\leq$5:1

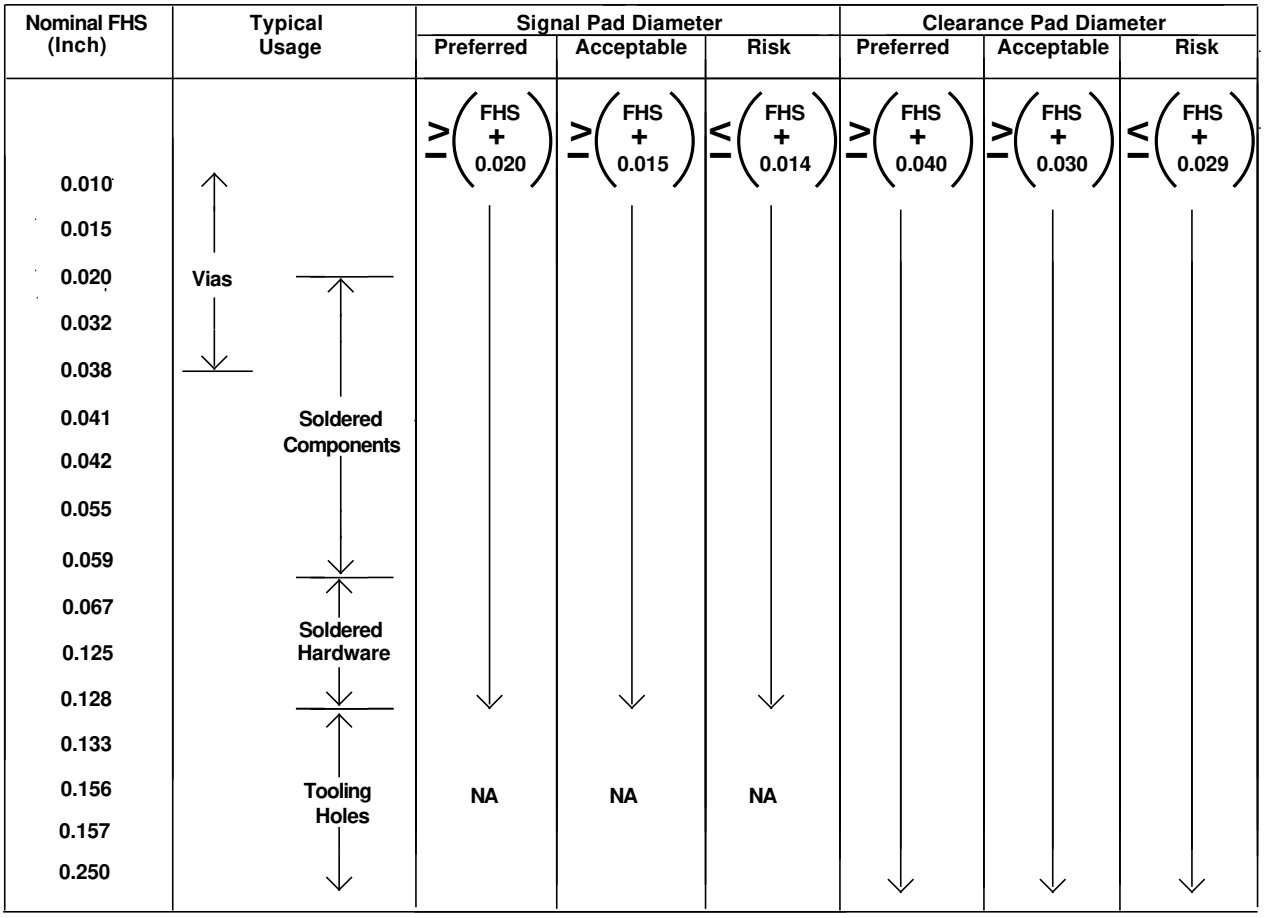
b. Acceptable - 6:1 to 9:1

c. Risk - $\geq$10:1

RULE 4014: OVERALL BOARD THICKNESS/COMPONENT LEAD LENGTH

The overall board thickness, inclusive of soldermask, must be considered when selecting components to meet the lead length requirements of EL-SM116-01, *Manufacturing Workmanship Standards and Related Documents: Workmanship Standards - Volume 1.*

Exhibit 1: Standard Signal Pad and Inner Layer Clearance Pad Diameters



RULE 4020: SELECTION OF MINIMUM NOMINAL LINE WIDTH

Nominal conductor etch line widths not subject to functional restrictions (such as current carrying capability, signal integrity, and so forth) shall be selected as follows.

Minimum Outer Layer Line Width

a. Preferred - ≥0.008 inch

b. Acceptable - ≥0.005 inch

c. Risk - < 0.005 inch

Minimum Inner Layer Line Width

a. Preferred - ≥0.006 inch

b. Acceptable - ≥0.005 inch

c. Risk - < 0.005 inch

RULE 4025: MINIMUM SPACING

Minimum spacings not subject to functional restrictions (such as product safety, signal integrity, and so forth) shall be routed **equally spaced** as follows.

Minimum Outer Layer Spacing

a. Preferred - ≥0.010 inch

b. Acceptable - ≥0.007 inch

c. Risk - < 0.007 inch

Minimum Inner Layer Spacing

a. Preferred - ≥0.008 inch

b. Acceptable - ≥0.006 inch

c. Risk - < 0.006 inch

3 PWB DESIGN RULES

PWB design rules and requirements pertaining to the following are provided under this heading.

a. Marking features

b. Screened nomenclature

c. Copper weight and thickness

d. Grid layout

e. Soldermask

f. Multisignal layups

g. Design optimization

3.1 REQUIRED MARKING FEATURES

Exhibit 2 lists the rules for marking features for printed-wiring boards, modules, and backplanes. Marking will be in etch whenever possible. When not possible, the more costly screened nomenclature is an acceptable alternative.

RULE 4100: COMPONENT REFERENCE DESIGNATORS

Whether marked in etch or silk screen, nomenclature for all component reference designators shall be in accordance with DEC STD 056-3.

RULE 4180: MINIMUM MARKING LINE WIDTH FOR ETCH

Minimum line width requirements for acceptable marking visibility are as follows.

- For base copper foil weights less than or equal to ½ oz, the line width shall be 0.008 inch.
- For base copper foil weights greater than ½ ounce but less than or equal to 1 ounce, the line width shall be 0.010 inch.
- For base copper foil weights greater than 1 ounce, the line width shall be 0.012 inch.

Exhibit 2: Rules for Required Marking Features

RULE NO.	FEATURE	EXAMPLE	APPLICATION				
			DBASE	ETCH	SMASK	SCREEN	SEE NOTE
2090 (ref.)	Product Safety Frames and Markings	digital™	✓	✓	—	×	1
2100 (ref.)	Copyright and Mask Works Protection Markings	Ⓜ© 1989 DIGITAL EQUIPMENT CORP. ALL RIGHTS RESERVED	✓	✓	—	×	5
4070	PWB Part Number and Revision Number (etch layers only)	50–12345–01 B01 Side 1 preferred, Side 2 acceptable. Required on all other etch layers.	✓	✓	—	—	2
1085 (ref.)	Crop Marks	(ONLY on corners where standard tooling is NOT provided.)	✓	✓	—	—	3
4140	Layer ID (etch layers only)	L1, L2, etc.	✓	✓	—	—	4
	Ground/Power Plane ID	GND, PWR					
	Power Potential ID	+5V, –3V, –12V, etc.					

KEY: ✓ = REQUIRED — = NOT APPLICABLE × = ALTERNATIVE (only when etch is not possible)

These markings are required within the circuit area unless otherwise specified.
Note 1. See DEC STD 030-2, Rule 2090 for details.
Note 2. See *DEC STD 012-0 Part Identification Standard*.
Note 3. See DEC STD 030-1, Rule 1085 for details.
Note 4. Layer ID shall read right from side 1 through to center of the board, and read right from side 2 on the remaining layers. If there is an odd number of layers, the center layer shall read right from side 2.
Note 5. See DEC STD 030-2, Rule 2100 for details.

RULE NO.	FEATURE	EXAMPLE	APPLICATION				
			DBASE	ETCH	SMASK	SCREEN	SEE NOTE
4150	Negative Plot Symbol (minimum dimensions)	(0.200–inch outer square) (0.100–inch inner square) (on all negative artwork)	✓	✓	—	—	—
4160	Module Number	54–12346, R284, M6543 (Must remain visible after assembly)	✓	✓	—	X	—
PREFERRED BUT NOT REQUIRED — When using any of the following preferred features, the applications shown are required.							
Functional Title		32K MOS mem	✓	✓	—	X	—
Discrete Reference Designator		R4, C9, D4, Q7	✓	✓	—	X	—
IC Designator		E1, E2 (Data base and etch on component side near handle or top of each row.)	✓	✓	—	X	—
Pin 1 Indicator (ETCH)		Round pad replaced by square pad of equal dimensions, both sides of PTH. Place on dispersion via for SMT.	✓	✓	—	—	—
Pin 1 Indicator (SCREENED)		If indicator not possible in etch, place an isosceles triangle adjacent to and pointing at appropriate feature.	✓	—	—	✓	—
Polarity Indicators (etch or screened)		+ symbol at capacitor anode – symbol at diode cathode	X	X	—	X	—

KEY: ✓ = REQUIRED — = NOT APPLICABLE X = ALTERNATIVE (only when etch is not possible)

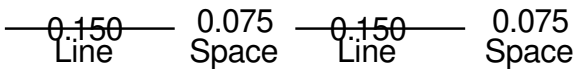
These markings are required within the circuit area unless otherwise specified.

3.2 SCREENED NOMENCLATURE REQUIREMENTS

Marking will be in etch whenever possible. When not possible, the more costly screened nomenclature is an acceptable alternative. Additional cost is due to increased process tolerance issues. Contact the owner of this section of DEC STD 030 for details before proceeding.

RULE 4181: SCREENED NOMENCLATURE - COMPONENT OUTLINES

Do not use component outlines unless specifically required by the design documentation. Component outlines, if required, shall be shown in the approximate size, shape, and orientation of the component and shall meet clearance requirements. For line lengths greater than 0.150, broken lines are preferred to solid lines. For example,



RULE 4182: SCREENED NOMENCLATURE - LINE WIDTH

The minimum line width of nomenclature shall be 0.012 inch.

RULE 4183: SCREENED NOMENCLATURE - LETTERING HEIGHT/WIDTH

Text shall be 0.060 inch minimum (letter height) and, as reference designators, shall be placed adjacent to the component so as to be visible after assembly. Text width shall be consistent with the font determined by the height requirement.

RULE 4184: SCREENED NOMENCLATURE - CLEARANCE REQUIREMENTS

Nomenclature features shall have 0.015-inch minimum edge-to-edge clearance from exposed terminal areas and functional access locations (for example, component pads, ESD tabs, fingers, test pads, vias).

RULE 4185: SCREENED NOMENCLATURE–ALIGNMENT MARKINGS

In order to provide accurate registration of screened nomenclature to the PWB, a minimum of two alignment markings are necessary. The symbol for the alignment markings shall be a + meeting all line width, lettering height, and clearance requirements. The symbols shall be located on diagonally opposite corners of the circuit when space permits.

The exact location and physical geometry of the symbols shall be provided in the product design data and in the corresponding silk screen layer data for each external etch layer to be silk screened.

The symbols that are etched on the external layers are then used to accurately align the corresponding symbols on the nomenclature layers.

3.3 FINGERED BOARDS

Guidelines and rules that apply to fingered boards are included under this subhead.

3.3.1 Guidelines for Deleting Unnecessary Fingers

Gold fingers should not be deleted unless there are more than three adjacent fingers per set that are unused on one side of the board. If fingers *are* left in a set, at least fingers A and V must remain in each finger set.

3.3.2 Rules for Fingered Boards

The following rules apply to fingered boards. See drawing K-DD-ELEN600-0-0 in EL-ENPCB-01, *PC Board Engineering Handbook—Standard Circuit and Finger Detail Drawings*, for a drawing example.

RULE 4190: STANDARD POWER AND GROUND FINGER ASSIGNMENTS FOR 0.125-INCH FINGERS

Unless otherwise specified:

Ground	=	Fingers C2 and T1
+5 Vdc	=	Finger A2
-15 Vdc	=	Finger B2

Where possible, these fingers shall be extended to a double pad as shown in Exhibit 3 and connected, where applicable, directly to the inner layer plane without a thermal impedance pad. This will minimize voltage drop.

RULE 4200: RESTRICTED FINGERS FOR 0.125-INCH FINGERS

Do not use fingers U1 or V1 unless necessary or specified. If the module were installed incorrectly, power would be supplied to these fingers.

RULE 4210: SPARE FINGERS

If spare fingers are desired, extend and terminate at via pads for both side 1 and side 2. The engineer shall specify which fingers should be extended as spares. Refer to Exhibit 3.

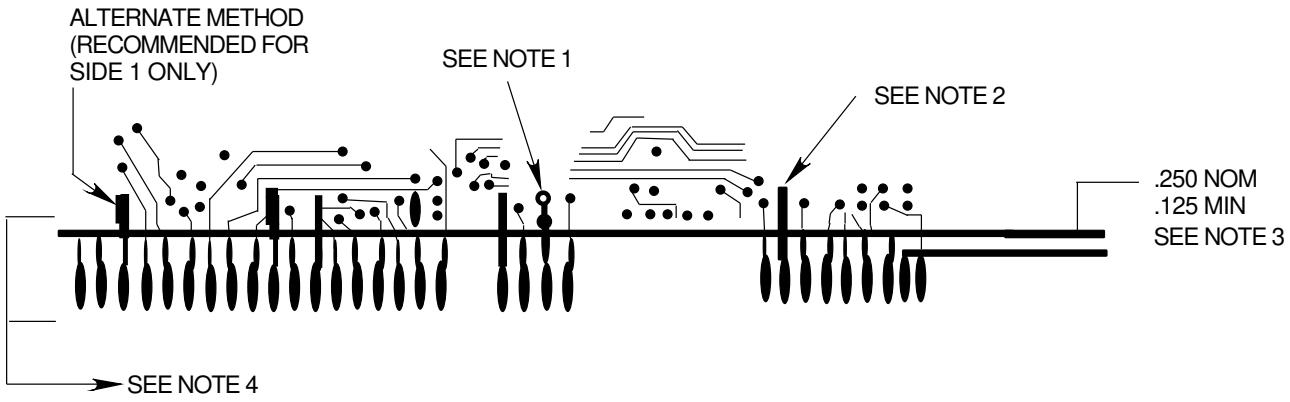
RULE 4220: STANDARD CONNECTOR AND FINGER DESIGNATIONS

Connector and finger designations are standard for each plug-in board type and are identified in accordance with *DEC STD 056-0 Symbology - Circuit Schematic Requirements*. Refer to DEC STD 030-1, Exhibit 15 for proper reference drawings.

RULE 4230: SPACING BETWEEN FINGERS AND PADS

Wherever possible, maintain a 0.25-inch space between the end of a connector finger and any pad. The minimum space allowed is 0.125 inch. Refer to Exhibit 3.

Exhibit 3: Extension of Standard and Spare Connector Fingers



Note 1. See Rule 4190.
Note 2. See Rule 4210.
Note 3. See Rule 4230.
Note 4. See Rule 4240.

RULE 4240: CONDUCTORS IN GOLD-PLATED AREA

Do not place etch in any area of the printed-wiring board that will be gold-plated (that is, below the top of the finger line). For T-series modules, see the VAXBI™ drawings T1999 and T1996.

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3.4 COPPER WEIGHT/THICKNESS

RULE 4250: COPPER WEIGHT - POWER/REFERENCE (GROUND) PLANE LAYERS

One ounce (0.0014-inch nominal) is the preferred copper weight for power/reference (ground) plane layers. Before deciding on a copper weight greater than 1 ounce for a new design (or substituting a 1-ounce copper weight for an existing design with copper weight greater than 1 ounce), the product engineer and logic designer should verify the chosen weight. The guidelines for verification are defined in DEC STD 030-1, Appendix A, and EL-ENPCD-TM, *Electrical Design Guide for Printed Circuits*. Avoid using copper weights greater than 3 ounces on inner layer power/reference planes. See *EL-ENPCB-02 PC Board Engineering Handbook—Layer Construction Drawings* for layer construction detail drawings.

RULE 4260: COPPER WEIGHT - INNER LAYER SIGNAL LAYERS

For internal signal layers, the base copper foil must meet the preferred copper weight for the signal technology used. One ounce (0.0014-inch nominal) is the preferred copper weight for all 5/5, 6/10, 8/8, and 12/13 inner signal layer technologies. Avoid using copper weights greater than 2 ounces on inner signal layers. Refer to EL-ENPCB-02 for detail drawings.

RULE 4267: UNEVEN COPPER WEIGHT

Equal copper weight on each side of a laminate core is preferred. When uneven copper weight is required for functional design reasons, the copper foil weight of each layer on a single laminate core used in a multilayer construction shall not differ by more than 1 ounce.

RULE 4268: USE OF CLASS III COPPER FOIL

Electrodeposited copper foil meeting ANSI/IPC CF-150 Class III requirements is required for designs greater than or equal to 10 layers fabricated from base laminate materials with resin glass transition temperatures (Tg) less than 200° C. Designs fabricated with laminate base materials whose resin Tg is greater than or equal to 200° C should use electrodeposited foil meeting ANSI/IPC CF-150 Class I, regardless of layer count.

RULE 4270: COPPER WEIGHT - OUTER LAYERS

Copper weight is determined by the minimum design line width. The following starting copper weights are required.

- For designs with minimum line widths less than or equal to 0.012 inch, 0.5-ounce (0.0007-inch nominal) copper foil shall be used.
- For designs with minimum line widths from 0.013-inch through 0.020-inch, 1-ounce (0.0014-inch nominal) copper foil may be used.
- For designs with minimum line widths greater than 0.020 inch, 2-ounce (0.0028-inch nominal) copper foil may be used.
- Avoid using copper foil weights greater than 2 ounces on external layers.

See DEC STD 030-8, Rule 8060, Rule 8070, and Rule 8080.

NOTE

The finished line width depends on the base foil thickness and etch factor in the PWB process. Line width is reduced by approximately two times the base foil thickness.

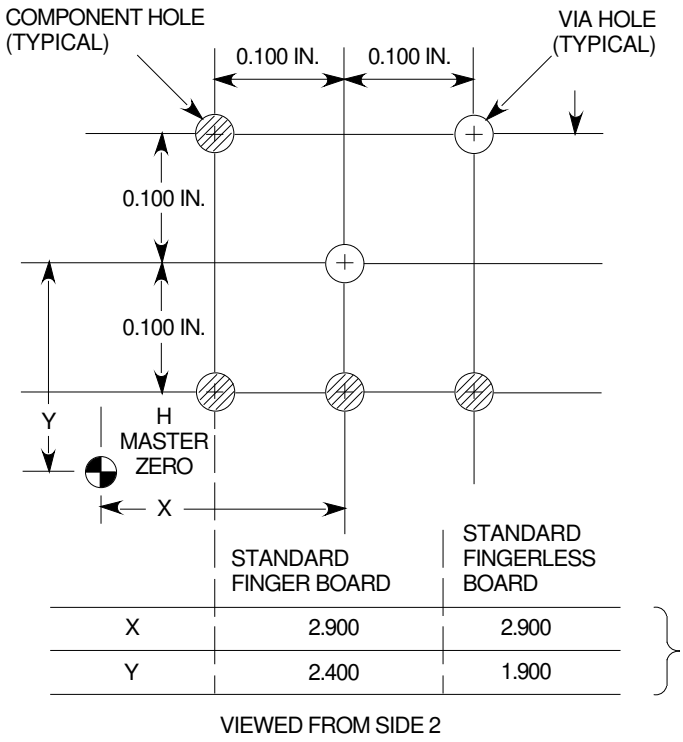
3.5 GRID RULES/BARE BOARD TEST

Rules for grid layout, bare board test, and component/via spacing are included in this heading. The bare board test rules address the test process for all PWBs as well as that for boards encompassing surface mount technology and planar resistor technology.

3.5.1 Grid Definition

A standard grid layout pattern is a pattern where component leads and vias are located on a 0.100 inch by 0.100 inch fixed grid relative to H-master zero. See Exhibit 4. Vias may also be located on different grids with respect to the same 0.100 inch by 0.100 inch fixed grid pattern, provided feature spacings are maintained. Test fixtures are not required for the standard grid layout pattern, provided a universal grid tester is available.

Exhibit 4: Standard Grid Layout of Component Lead Holes and Vias on 0.100-Inch by 0.100-Inch Depopulated Grid



	STANDARD FINGER BOARD	STANDARD FINGERLESS BOARD	
X	2.900	2.900	POSITION OF THE FIRST AVAILABLE COMPONENT HOLE
Y	2.400	1.900	

VIEWED FROM SIDE 2

NOTE

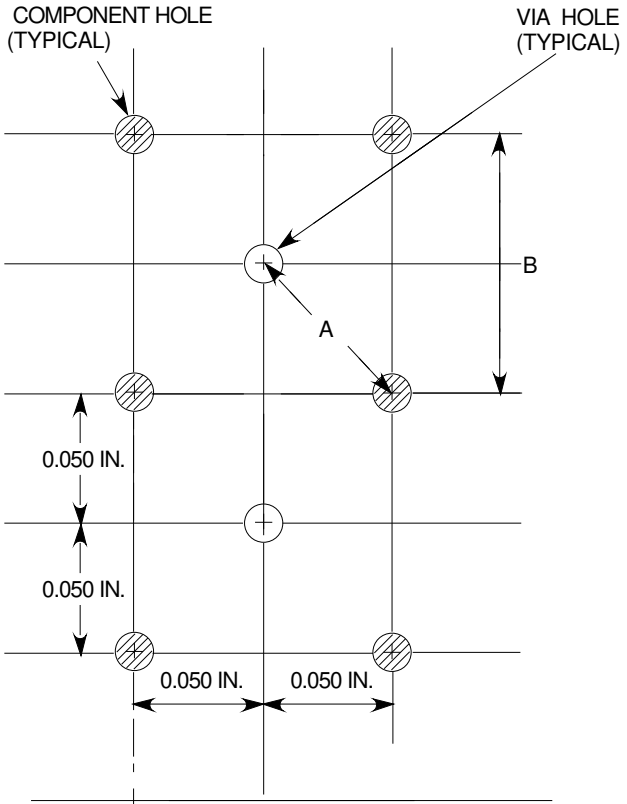
When possible, the standard grid layout pattern shall be applied to all of Digital's PWB products to help ensure the lowest possible unit transfer cost and fastest volume deliveries.

For any density board, vias placed on standard grid are recommended.

A staggered grid layout pattern is a pattern where component leads are located on a 0.100 inch by 0.100 inch fixed grid pattern, but vias are allowed to be located on increments of 0.050 inch by 0.050 inch and 0.050 inch by 0.100 inch with respect to the same 0.100 inch by 0.100 inch fixed grid pattern. See Exhibit 5. This layout pattern allows greater test point density, but requires the fabrication of a product-specific test fixture.

Refer to DEC STD 030-6 and *DEC STD 140-1 Documentation Requirements for Printed-Wiring Boards (50-Class)* for additional information on bare board and module test requirements.

Exhibit 5: Staggered Grid Layout of Component Lead Holes and Vias



A	0.070 IN. CENTER–TO–CENTER
B	0.100 IN. CENTER–TO–CENTER

3.5.2 Bare Board Test

Rules 4290 through 4320 apply to the bare board test process for all PWBs. Refer to Section 3.5.2.1 and Section 3.5.2.2 for those rules applicable to testing of boards encompassing surface mount and planar resistor technologies, respectively.

RULE 4290: TEST POINT DENSITY

Density of test points shall not exceed 200 points per square inch, with 0.050-inch minimum spacing between test points. For designs with density greater than 200 points per square inch, contact the Corporate PWB Group Quality Manager to discuss test process changes.

RULE 4300: TESTABILITY

Verify that the design data allows continuity test fixturing access to 100 percent of networks.

Any product that does not comply with Rule 4300 requires a waiver from the Corporate PWB Group Quality Manager.

Products can be delayed several weeks if the test data does not contain accurate network information. Data-driven test is the ultimate goal, reducing timely data verification procedures. This concept should be fully considered at the design level.

RULE 4315: HIPOT TESTING

HIPOT testing of power-to-ground planes is required on all PWBs of 8 layers or more. The recommended contacts are the power tab/finger vias or the bypass capacitor mounting holes.

Avoid placing surface etch features connected to inner layer planes (PWR, GND, REF) within 0.050 inch of each other. When HIPOT testing at 1000 Vdc, exposed surface features with a 1000 Vdc difference in potential (power and ground feature) are subject to surface arcing (in air) if the distance between the points is less than 0.050 inch. Consideration of this breakdown limitation must be taken into account during design layout.

Any plane to which a planar resistor is attached shall not be identified for HIPOT testing, to prevent damage to resistors.

RULE 4320: COMPONENT HOLES DESCRIBED AS VIAS IN THE PWB DATA BASE

Component holes shall not be described as vias in the PWB data base. This may lead to problems in the board fabrication and assembly test processes.

The placement of vias within SMT pads is currently being researched. Consult the owner of this section of DEC STD 030 for the most current data.

3.5.2.1 Surface Mount Technology (SMT)

RULE 4321: SMT FOOTPRINT DISPERSION ETCH VIAS

All footprint dispersion etch vias shall be placed on a grid appropriate for the components being used.

The placement of vias within SMT pads is currently being researched. Consult the owner of this section of DEC STD 030 for the most current data.

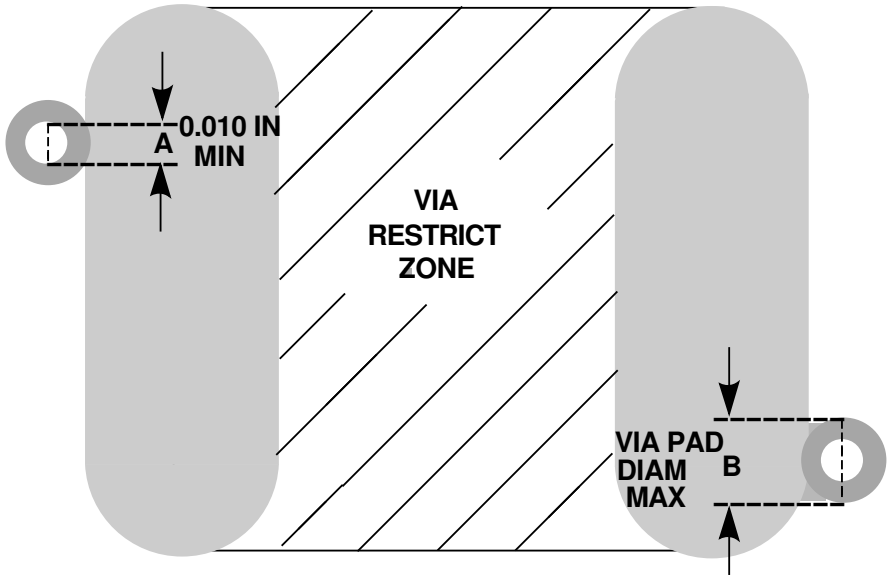
RULE 4322: USE OF TANGENTIAL VIAS WITH PASSIVE CHIP COMPONENTS

The following list identifies the application and describes the features of tangential vias.

- Application: Passive chip components **ONLY**.
- Description: Via pad tangent to SMT pad. Refer to Exhibit 6.

  Minimum via pad to SMT pad contact area: 0.010 inch (dimension A in Exhibit 6). Maximum via pad to SMT pad contact area: via pad diameter (dimension B in Exhibit 6).
- Location: Tangential vias not allowed within the interior of the pad pattern as shown in the restricted zone of Exhibit 6. Refer to DEC STD 030-5, Rule 5710.
- Via FHS: 0.010 inch minimum to 0.020 inch maximum.
- Aspect ratio: Within the values stated in Rule 4012.
- Pad size: As stated in Rule 4010.
- Soldermask: Refer to Rule 4535 and Rule 4545.

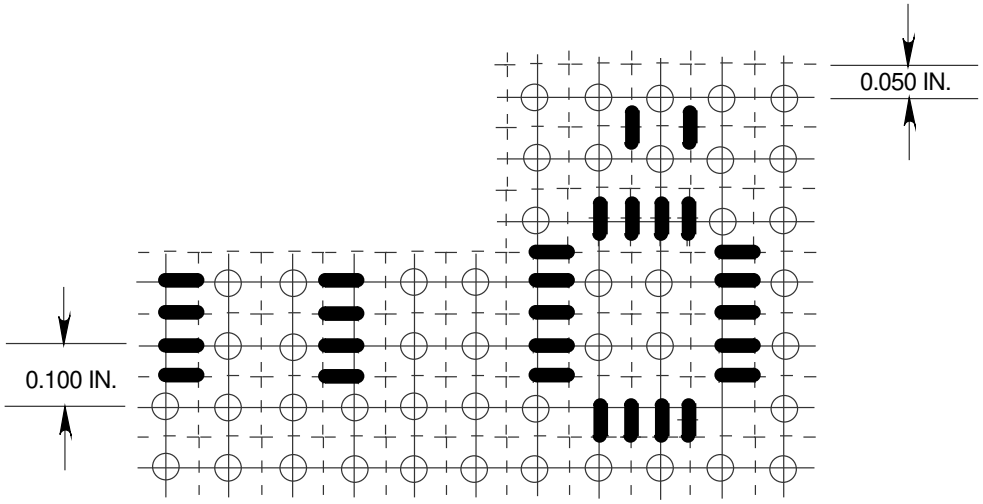
Exhibit 6: Tangential Vias



RULE 4323: SURFACE MOUNT TEST GRIDDING

Surface mount devices shall be placed so that their footprints lie along and across a 0.050-inch grid that coincides with the 0.100-inch via grid. This condition allows maximum coverage with the 0.050-inch pitch used for bare board test points. See Exhibit 7.

Exhibit 7: Surface Mount Test Via Gridding



RULE 4324: END POINT TESTING

Quality goals require that bare boards be electrically tested to all end points to ensure that the PWB is free of shorts and opens.

All surface mount pads of 0.025-inch pitch or greater are defined as *end points* and shall be tested for electrical continuity at the completed bare board level. Surface mount pads with less than 0.025-inch pitch shall be electrically tested to the dispersion etch via with automated optical inspection from the via to the end of the SMT pad.

RULE 4325: DRILLING LOCATION FOR BARE BOARD TEST FIXTURE

The exact center of the surface mount pad shall be located in the data base so that the correct drilling location for the bare board test fixture can be located. Components with 0.025-inch pitch require offset test points within the pad to allow for the staggering of the test probes within the surface mount pad field.

3.5.2.2 Planar Resistor Technology (PRT)

RULE 4326: PLANAR RESISTOR CONFIGURATION

The configuration of each planar resistor shall be identified as either series or parallel.

RULE 4327: PLANAR RESISTOR LOCATION/ALTERNATE TEST POINT

The X-Y location and its alternate test point shall be identified for each planar resistor.

RULE 4328: FINISHED PLANAR RESISTOR VALUE AND TOLERANCE

When a design requires planar resistor technology, a separate sheet shall be included in the MD set for each PRT layer, showing the planar resistors viewed from side 1.

A CAD file shall also be provided that defines the following information for each resistor.

- Resistor value expressed in ohms
- Resistor high tolerance expressed as a percent
- Resistor low tolerance expressed as a percent
- Layer name of the resistive layer
- Reference designator for the resistor under test (see *DEC STD 056-3 Symbology - Discrete Electronic and Electromechanical Component Symbols*)
- Test point locations for the resistor (primary and alternate)

3.5.3 Component/Via Spacing Requirements

RULE 4330: COMPONENT LEAD SPACING

All new product module layouts must have component lead locations placed on a standard grid. When component leads cannot be placed ongrid because of footprint design or size, then the pin 1 location must be ongrid.

RULE 4340: COMPONENT HOLE-TO-VIA AND VIA-TO-VIA HOLE SPACING

Pad-edge to pad-edge spacing for components-to-vias or vias-to-vias shall be greater than or equal to 0.015 inch unless at least one via is tented. Refer to DEC STD 030-5, Rule 5147 for soldermask requirements.

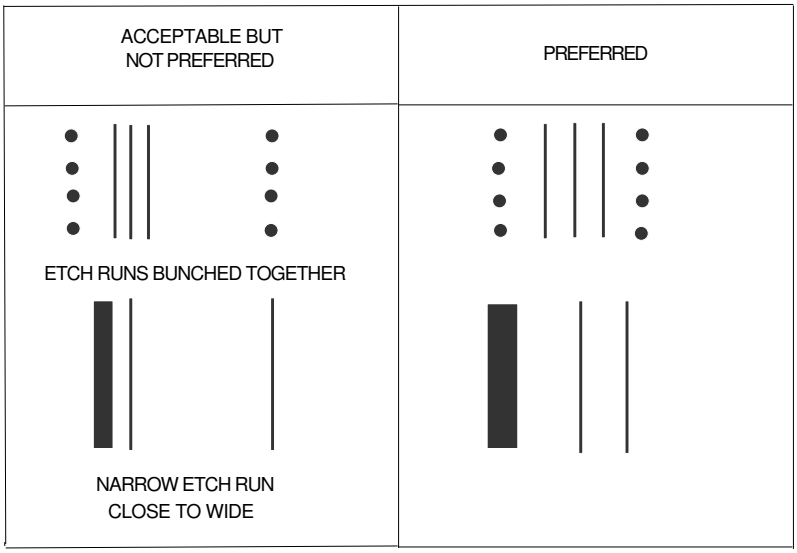
3.6 DESIGN OPTIMIZATION RULES

Guidelines and rules for achieving design optimization are included under this heading.

RULE 4370: CONDUCTOR SPACING

Equalize and maximize conductor spacing within the routing area whenever possible on external layers. This will increase yields and reduce scrap. Refer to Exhibit 8.

Exhibit 8: Conductor Spacing



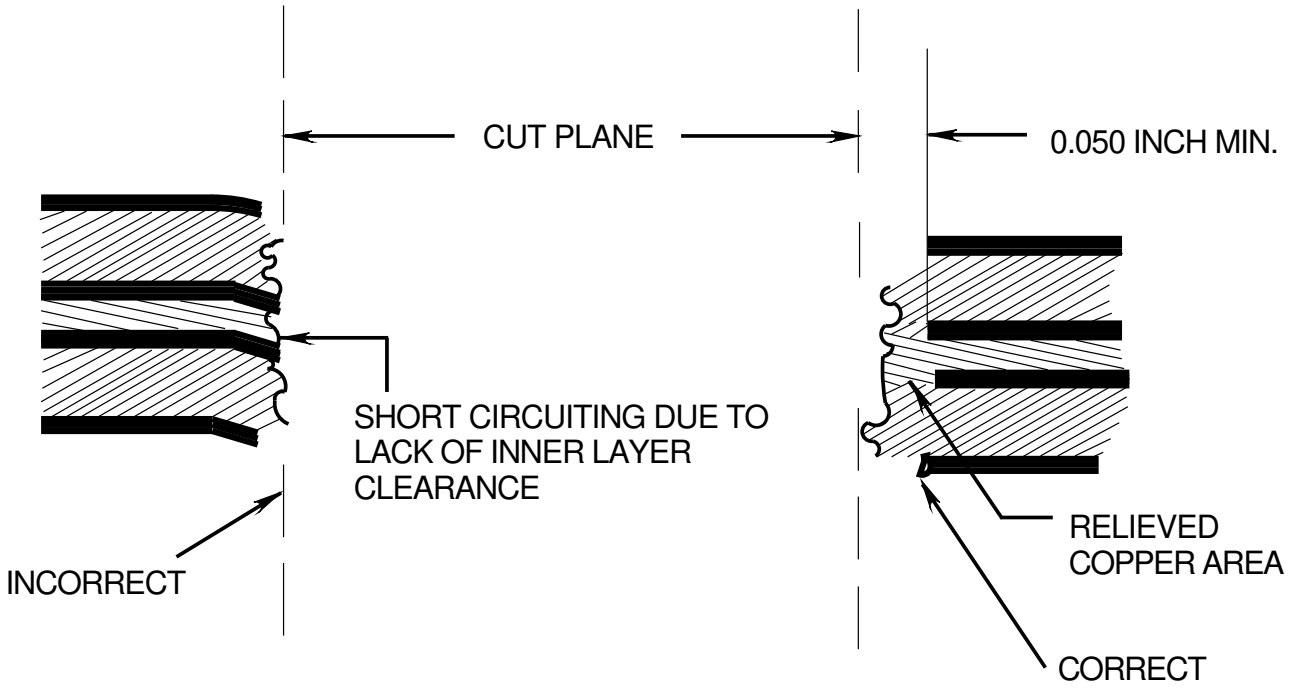
RULE 4390: SPACING OF PAD, CONDUCTOR, OR INNER LAYER PLANE TO BOARD EDGE OR CUTOUTS

The distance from a pad, conductor, or inner layer plane to the board edge or cutouts shall be 0.050-inch minimum. Nonfunctional copper (for example, crop marks or autothieving) shall be placed 0.025-inch minimum from the circuit edge.

Whenever a multilayer board is sheared, routed, or punched, the affected areas on all layers must be free of copper. For instance, inner layers must be relieved from the cut surface (on the artwork) to prevent a short circuit. Refer to Exhibit 9.

If cutting through a copper plane cannot be avoided, be sure that there is no copper on the adjacent layer in the affected area (as shown in Exhibit 9) and that conductive hardware cannot under any circumstances come in contact with the exposed inner layer copper.

Exhibit 9: Inner Layer Conductor Relief from Edges for Isolation



RULE 4392: DISPERSION ETCH DIMENSIONS AND INNER LAYER ROUTING - COMPATIBLE COMBINATIONS

The dimensions of dispersion etch, surface mount component pads, and vias must be selected in a compatible combination. Exhibit 10 lists suggested combinations. Etch may connect directly to other features without the use of vias. As with any design, the use of larger size features, when space permits, can lead to improved reliability and manufacturability.

The placement of vias within SMT pads is currently being researched. Consult the owner of this section of DEC STD 030 for the most current data.

Exhibit 10: Suggested Dispersion Etch Dimensions and Inner Layer Routing Compatible Combinations (Inches)

Lead Pitch	Dispersion Etch Width	Typical* Footprint Pad Size	Inner Layer Etch Width	Inner/Outer Layer Via Pad		Typical Via Hole Size	
				0.100 Grid	0.050 Grid	0.100 Grid	0.050 Grid
0.050 0.025	0.010 0.005	0.030 x 0.076 0.016 x 0.076	0.006 0.005	0.040 0.025	0.025 0.025	0.020 0.010	0.010 0.010

* Refer to DEC STD 030-10, heading 3.

RULE 4395: TELEPHONE LINE ETCH SPACING

- On connectors where telephone signals are present, adjacent pins shall not be used if there is less than 0.200-inch spacing between signals, including component pads. In some cases, more than one pin may be unusable if accumulated distance is less than 0.200 inch between pins.
- Etch shall be placed 0.200 inch from mounting holes. The distance should be measured from the mounting device's maximum diameter and not the hole diameter since the device could be a screw or rivet that is wider than the mounting hole.
- On the module layout, etch carrying telephone signals shall be a minimum of 0.020 inch, with a minimum spacing of 0.040 inch between them. Etch shall also be spaced a minimum of 0.200 inch away from any conductive material such as handles and edge guides.

RULE 4400: NPTH TO CIRCUIT EDGE SPACING

Spacing of NPTH to circuit edge shall be greater than or equal to the board thickness.

RULE 4410: SPACING REQUIREMENTS FOR NPTH- TO-CONDUCTOR OR -PAD

Spacing between NPTH to conductor or pad must be a minimum of 0.020 inch on the outer layer except where governed by Rule 4390.

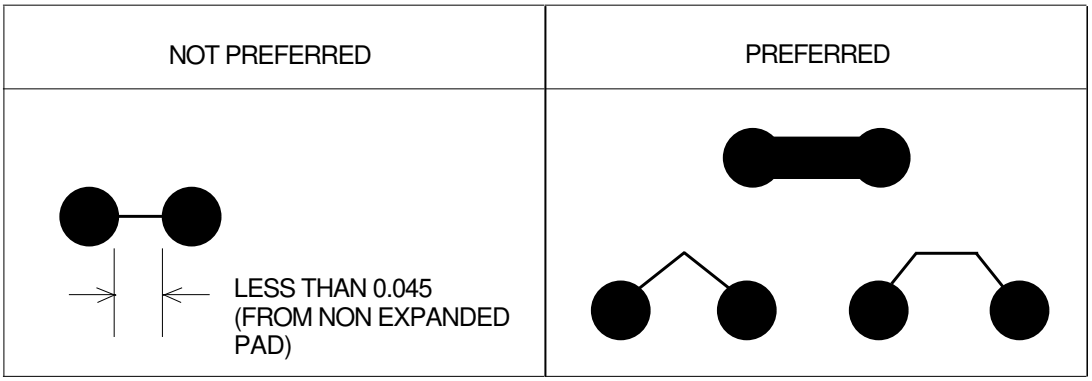
RULE 4420: SPACING REQUIREMENTS FOR NPTH-TO-NPTH

Spacing of NPTH to NPTH shall be greater than or equal to the board thickness.

RULE 4430: INTERCONNECTIONS BETWEEN ADJACENT PADS

Interconnections between adjacent pads on external layers must be more than 0.045 inch from pad to pad (before pad expansion). If the space is less than 0.045 inch, widen the etch. This will differentiate the connection from a solder short. The advantages of this will be reduced inspection problems and increased yields. See Exhibit 11.

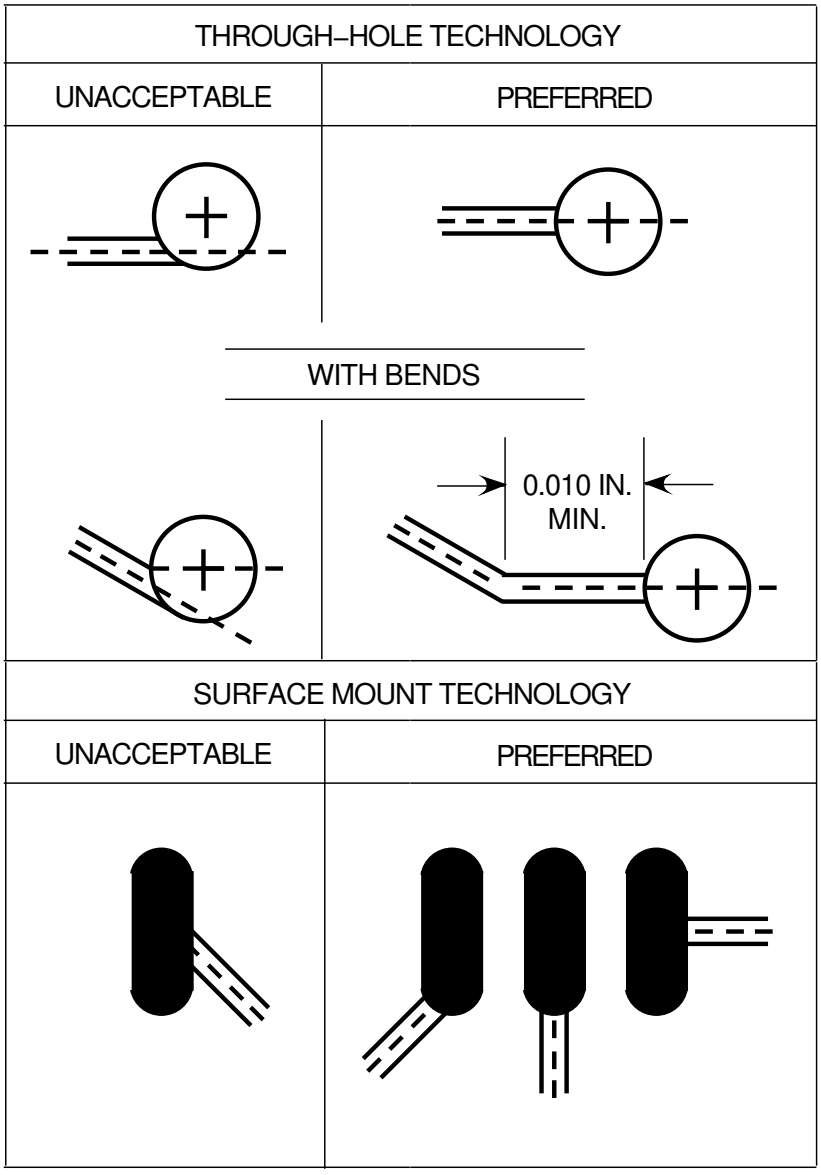
Exhibit 11: Interconnections Between Adjacent Pads



RULE 4440: INTERCONNECTIONS BETWEEN PADS AND LINES

Line-to-pad connections shall be placed such that the line is perpendicular to the arc of the pad (that is, the centerline axis of the line contains or passes through the center of the pad). Connections between component pads and passing conductors must be a minimum length of 0.050 inch. Spacing from edge of pad to bend point shall be 0.010 inch minimum to permit pad expansion. Angles less than 90 degrees are unacceptable for any technology. See Exhibit 12 through Exhibit 14.

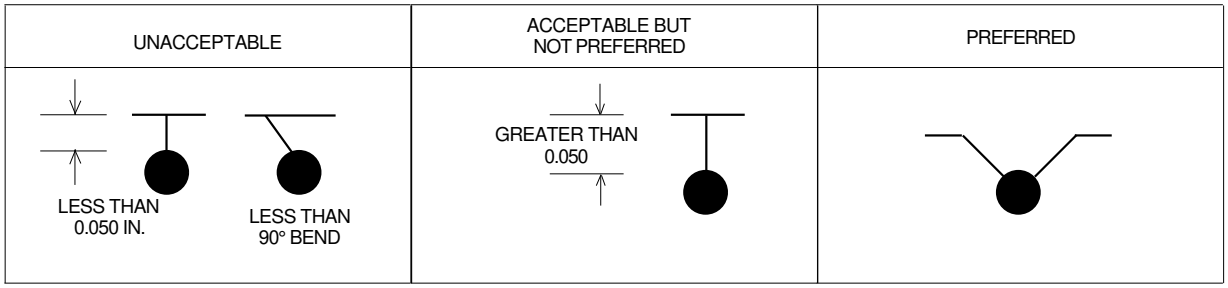
Exhibit 12: Interconnections Between Pads and Lines



RULE 4450: MINIMUM ANGLES WHEN ROUTING ETCH

Inside angles of less than 90 degrees are unacceptable for any technology. See Exhibit 13 and Exhibit 14.

Exhibit 13: Minimum Length of Interconnections Between Pads and Lines

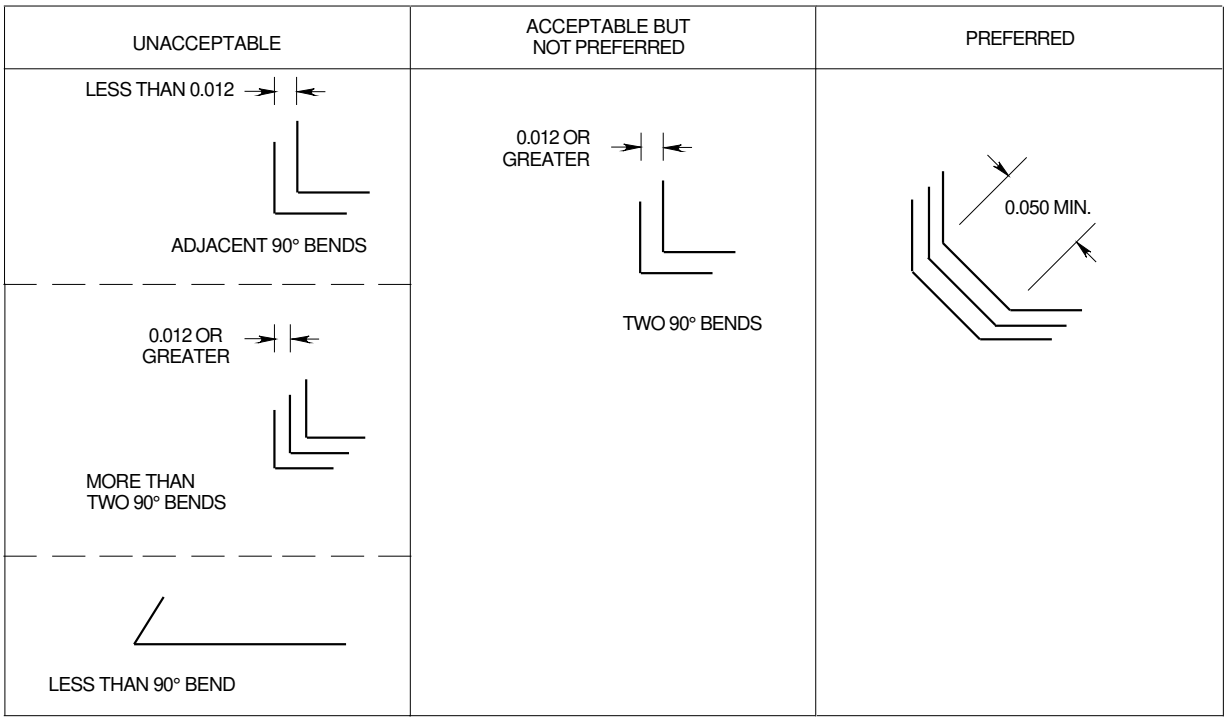


RULE 4460: 90-DEGREE BENDS — OUTER LAYER CONDUCTORS

Plated outer layer conductor lines with 90-degree bends are subject to the following criteria, as shown in Exhibit 14. The advantages of Rule 4460 are reduced solder shorts in the board shop and assembly, and the elimination of resist entrapment in corners.

- The preferred bend for all technologies is 45 degrees. However, manual rework is not required on previously created 90-degree bends on 0.012-inch spaces or greater. The 45-degree bends should be a part of the CAD system.
- At design layout, all PWBs with 0.012-inch spaces or greater may have 45- or 90-degree bends. Do not cluster more than two 90-degree bends together.
- All PWBs designed with less than 0.012-inch spaces between etch lines shall not have adjacent 90-degree bends.

Exhibit 14: 90-Degree Bends



RULE 4470: PAD EXPANSION (SIGNAL LAYERS)

Pad expansion is not required on outer layers. For inner signal layers, pad expansion is required where any line connects to a pad for all pad sizes on all signal layers. Do not expand the pad if the line width is greater than or equal to the expansion pad size. The following pad expansion sizes shall be used.

- For pads greater than or equal to 0.045 inch, pad expansion shall be 0.040 inch and may extend up to 0.0075 inch beyond the edge of the pad.
- For pads greater than or equal to 0.030 inch but less than 0.045 inch, pad expansion shall be 0.025 inch and may extend up to 0.0065 inch beyond the edge of the pad.
- For pads greater than or equal to 0.020 inch and less than or equal to 0.029 inch, pad expansion shall be 0.015 inch and may extend up to 0.0055 inch beyond the edge of the pad.

Other types of pad expansion are acceptable as long as they do not violate minimum spacing requirements.

RULE 4490: EQUALIZING DISTRIBUTION OF CONDUCTOR PATTERN

Conductors shall be distributed as evenly as possible over the entire board surface, including the outer edges, to minimize plating build-up where copper is concentrated (component side equal to solder side ± 20 %). Refer to Rule 4510 for size, placement, and distribution balance.

RULE 4510: AUTOTHIEVING (IN-CIRCUIT THIEVING) FOR PLATED SIGNAL LAYERS

A nonfunctional copper area is one that serves no functional purpose in the circuit. Nonfunctional copper should have a maximum width of 0.100 inch. Addition of nonfunctional copper may be used to provide balance and is normally necessary when large ground planes or enlarged voltage conductors are used.

Autothieving, or in-circuit thieving, is required for plated signal layers. Autothieving is a process that adds plating-current density sinks (nonfunctional copper) in a pattern across the circuit, and creates more uniform plating deposits and higher yields in the board shop. The design engineer must specify any areas to be void of thieving for functional reasons. Autothieving should be used on all prerelease prototypes to ensure that no functional impact or additional testing is required at release.

As a general rule, standard density (20/20), power supply designs, and HPWR backplanes may be autothieved if the requirements in EL-SM119-01, *Corporate Product Safety and Requirements - Volume 1 Information Processing and Business Equipment* are met.

A gross imbalance of surface copper conductor area or the need to provide tighter control of finished PTH sizes may require the use of autothieving for these designs. The decision to autothieve exceptions to Rule 4510 will be made by the owner of this section of DEC STD 030 in conjunction with the design engineer.

The following criteria shall be used to ensure equalized distribution of conductor pattern:

a. In-circuit thieving shall be added in any open area that is 2 square inches or larger.

b. Thieving must equal the circuit density of the surrounding area.

c. In-circuit thieving shall be added to board areas that can be cut from the panel when the final outline is formed.

d. To minimize plating buildup, in-circuit thieving shall be added around the perimeter of isolated circuit and pad features.

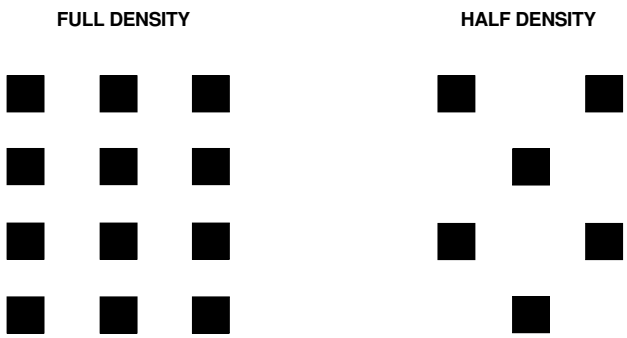
The autothieving algorithm runs on the following parameters.

a. Thieving shall be no closer to the circuit edge than 0.025 inch.

b. Thieving pads typically are 0.080-inch square on a 0.100-inch grid. Smaller autothieving feature sizes (such as 0.040 square inch) may be employed to overcome spacing violations and autothieving density limitations.

c. Thieving shall be full density within a 1.000-inch band inside the circuit outline, and half density over the remainder of the circuit. See Exhibit 15.

Exhibit 15: Full-Density Versus Half-Density Autothieving



d. No autothieving is allowed within 0.200 inch of any telephone line.

e. Standard Autothieving (SA) - Thieving pattern shall be no closer than 0.050 inch to any other feature or void area on products that do not require tighter impedance control on transmission lines.

f. Transmission Autothieving (TA) - The design engineer may choose to use TA for products that require tight impedance control. **If TA is required by the design engineer, it must be documented on the MD.**

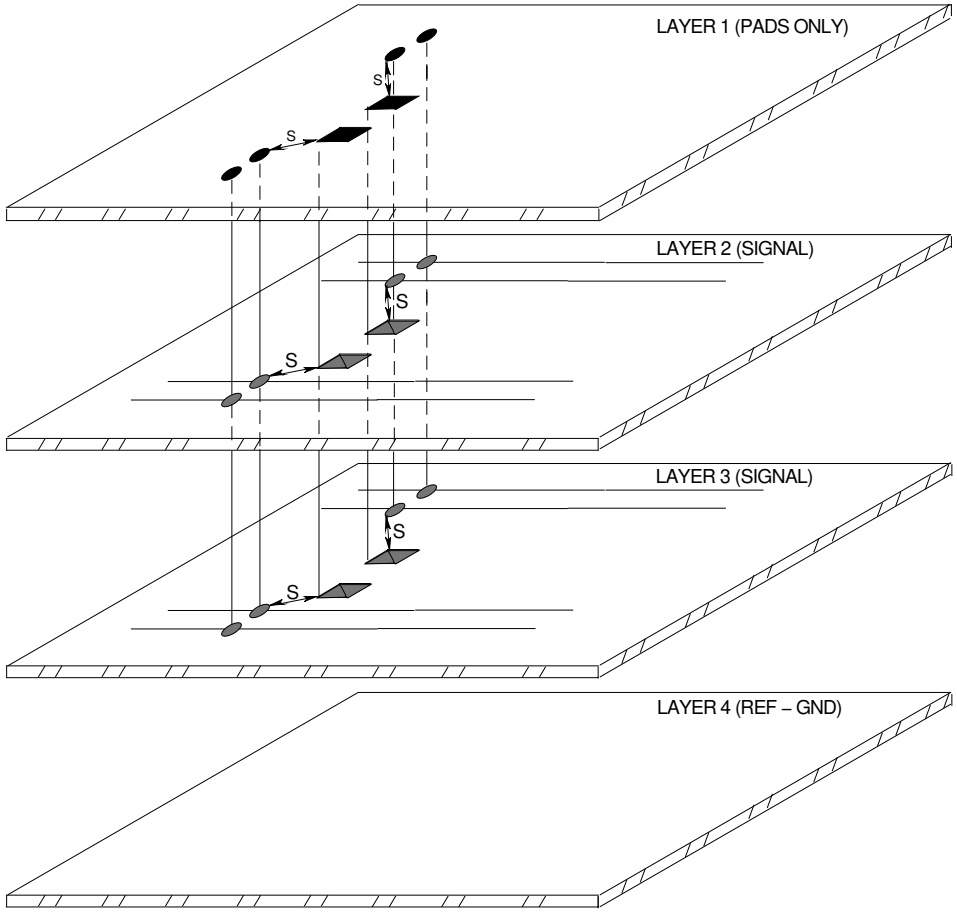
For TA, the outer layer thieving pattern must adhere to the following:

1. The outer layer thieving pattern shall be no closer than the minimum distance necessary for signal integrity to all adjacent outer layer features whose transmission line parameters (impedance and so forth) must be tightly controlled. This minimum distance must be determined by signal integrity analysis.
2. The outer layer thieving pattern shall be no closer than the minimum distance necessary for signal integrity to the transmission line features on all signal inner layers located above the outermost reference (ground) planes. This minimum distance shall be determined by signal integrity analysis. See Exhibit 16.

g. Transmission line products with signal inner layers "shielded" from outer layers, that is, within power or reference (ground) planes, are not subject to the restrictions in item f.2. In this instance, the outer layers shall use standard autothieving patterns whenever possible.

h. When signal integrity requirements preclude the use of an adequate level of autothieving, the physical size and location of autothieving features may be adjusted to provide sufficient copper area for uniform plating yet still comply with signal integrity requirements.

Exhibit 16: Spacing Requirements for Transmission Autothieving



S – TO BE DETERMINED BY SIGNAL INTEGRITY ANALYSIS.

3.7 SOLDERMASK RULES

Refer to DEC STD 030-5, heading 4.4 for soldermask assembly requirements.

Soldermask artwork dimensions are adjusted by the manufacturing post-processor. Soldermask artwork tools are based on the fabricator's soldermask capability. Final acceptance criteria is per *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*.

NOTE

Surface mount soldermask pad clearances depicted in EL-EN705-00, *Footprint Patterns for Surface Mount Technology* are offered as a diagrammatic aid and should not be interpreted as rules, particularly when they conflict with Rule 4535.

RULE 4535: SOLDERMASK CLEARANCE REQUIREMENTS

a. All conductive material shall be covered with soldermask except:

i As specified in other clauses to this rule.

ii Where it must be exposed in order to meet engineering design requirements.

iii Where it must be exposed in order to contact an already exposed area, such as when a trace connects an exposed area.

b. The design data dimensions for soldermask clearance and void areas shall be zero clearance, that is, identical to the nominal dimension of the circuit feature (pad or void areas). When rectangular void areas are used around SMT device footprints the zero clearance dimensions shall be the design data dimensions defined by the SMT footprint pad geometric configuration plus any additional clearance necessary for SMT assembly. **The PWB fabricator will provide the necessary adjustments in clearance to meet finished circuit requirements.** Refer to DEC STD 030-5, Rule 5149.

c. Soldermask shall be 0.020 inch from the circuit edge in order to encapsulate all surface etch.

d. Soldermask shall be 0.015 inch from the edge of a NPTH, cutout, or notch.

e. On solder-plated boards, soldermask shall not extend more than 0.025 inch onto any conductor area larger than 0.187 inch by 0.187 inch.

This does not apply to SMOBC and ALL COPPER. On SMOBC and ALL COPPER boards, all non-terminal surface etch must be covered with soldermask, except test pads and fiducials.

f. Component hole pads and assembly test pads shall be free of soldermask.

g. For gold fingers, soldermask shall extend to the top of the finger where the etch connection to the finger is made. All other areas shall be free of soldermask.

h. Any area that will have something soldered to it, such as fast-on tabs, shall be free of soldermask.

NOTE

UL block area (area designated for Julian Date Code) shall be covered by soldermask.

i. Areas designated for Electrostatic Sensitive Discharge (ESD) shall be free of soldermask.

j. For soldermask clearance around fiducials, refer to DEC STD 030-5, Rule 5800.

RULE 4540: MINIMUM SPACING–ETCH TO SOLDERMASK CLEARANCE VOID AREAS

Any surface metal feature intended to encapsulated by soldermask shall not be closer than 0.007 inch to any soldermask zero clearance or void area.

RULE 4545: MINIMUM SOLDERMASK WIDTH

The minimum width of soldermask material greater than 0.100 inch in length shall be:

0.025 inch with dry film soldermask
0.015 inch with all other types of soldermask

3.8 MULTILAYER REQUIREMENTS

Inner layer requirements, including the use of thermal impedance pads are included in the following rules.

RULE 4575: TELEPHONE ETCH AND INTERNAL LAYER CLEARANCES

All internal layers that are directly under telephone etch shall be free of copper.

RULE 4580: VENTING OF LARGE OPEN AREAS IN INNER LAYER COPPER PLANES

Openings in copper planes larger than 0.0625-square inch (equivalent to 0.250 inch by 0.250 inch) can cause air entrapment and delamination in board shop and assembly processing. If large open areas in copper planes are required, the following options shall be considered.

a. Vent the opening in the copper plane to the nearest circuit edge to allow volatile materials to escape during lamination. Consult the following table for vent stripe widths.

NOTE

Be aware that signal integrity of transmission lines passing over interrupted planes due to vent stripes will be affected.

Inner Layer Copper Vent Line	Vent Stripe Width (minimum)
3 oz.	0.093 inch
2 oz.	0.062 inch
1 oz.	0.031 inch

b. Depending on the geometry, place an area of nonfunctional copper within the opening in the copper plane. This area of nonfunctional copper shall be of sufficient size to maintain functional requirements and yield a minimum isolation to the plane of 0.020 inch.

c. If a plated-through hole is to be placed within the large opening in the copper plane, ensure the nonfunctional copper pad is at least 0.020 inch greater than the desired FHS, and the minimum isolation of the nonfunctional copper pad to the plane is 0.020 inch.

RULE 4600: USE OF THERMAL IMPEDANCE PADS

Thermal impedance pads are special pad configurations necessary where plated-through holes make a connection to an inner layer copper plane. This pad provides the means for preventing heat from dissipating into the inner layer instead of the solder joint. Connections to this plane shall be made with the standard thermal impedance pads (Exhibit 17), unless designs specifically require tighter controls on IR drop.

Failure to use the pads in these applications will usually result in PTH damage during component removal, poor solder fill during assembly, and difficulty in achieving PTH solder thickness and FHS requirements after reflow at bare board level. Exhibit 18 shows the thermal impedance pad to be used with VAXBI modules only. This pad has improved functional characteristics (IR drop, capacitance), but does not provide optimum solderability for other than VAXBI modules. Refer to EL-EN057-00 *VAXBI Module Layout Guide* for further information.

RULE 4605: FINISHED HOLE SIZE FOR VAXBI THERMAL IMPEDANCE PAD

VAXBI thermal impedance pads require a 0.038-inch finished hole size and can be used with either a via or component hole. Refer to Exhibit 18A .

Components requiring holes smaller than 0.038-inch must use a smaller version of the thermal impedance pad for improved routing capability. Refer to Exhibit 18B.

Exhibit 17: Standard Thermal Impedance Pads (Note: Drawings not to scale)

Exhibit 17A. Recommended for 0.100 Grid and Finished Hole Size ≤ 0..055 Inch

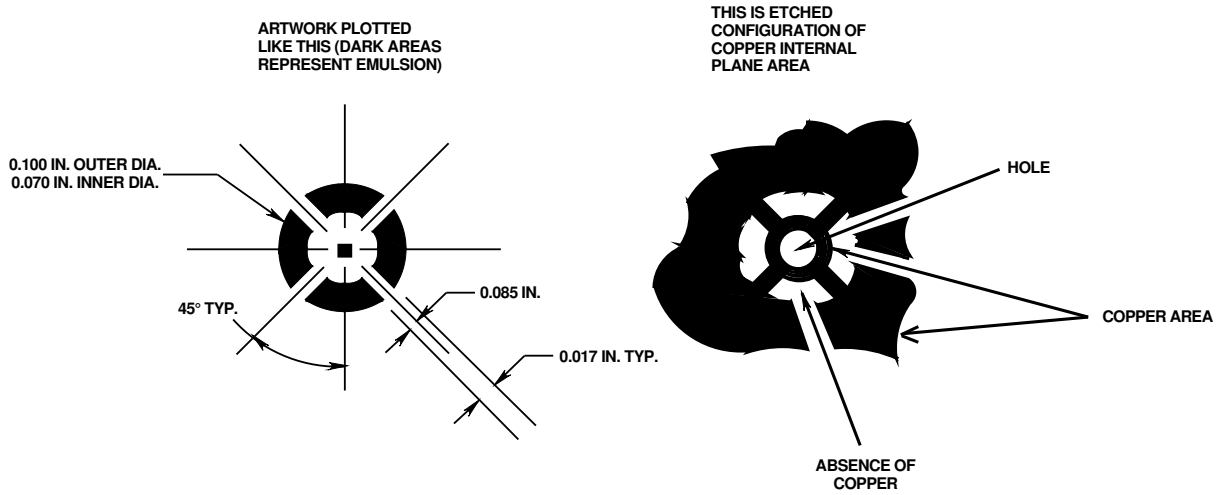


Exhibit 17B. Recommended for 0.100 Grid and Finished Hole Size ≤ 0..040 Inch for Improved Signal Integrity

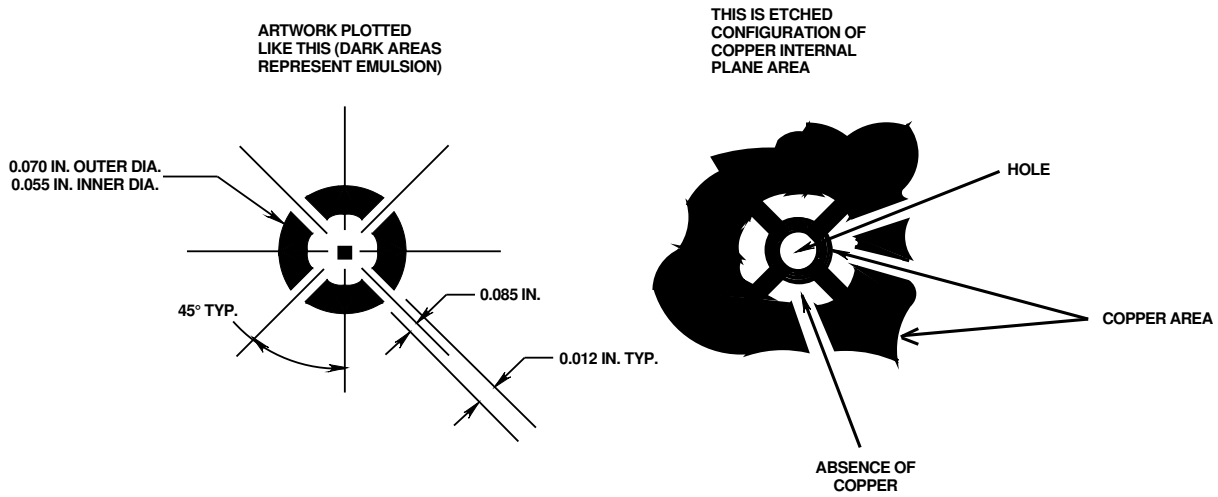


Exhibit 18: Thermal Impedance Pad for VAXBI Modules (Note: Drawings not to scale)

Exhibit 18A: Recommended for 0.100–Inch Grid and Finished Hold Size ≥ 0.038 Inch ≤ 0.055 Inch

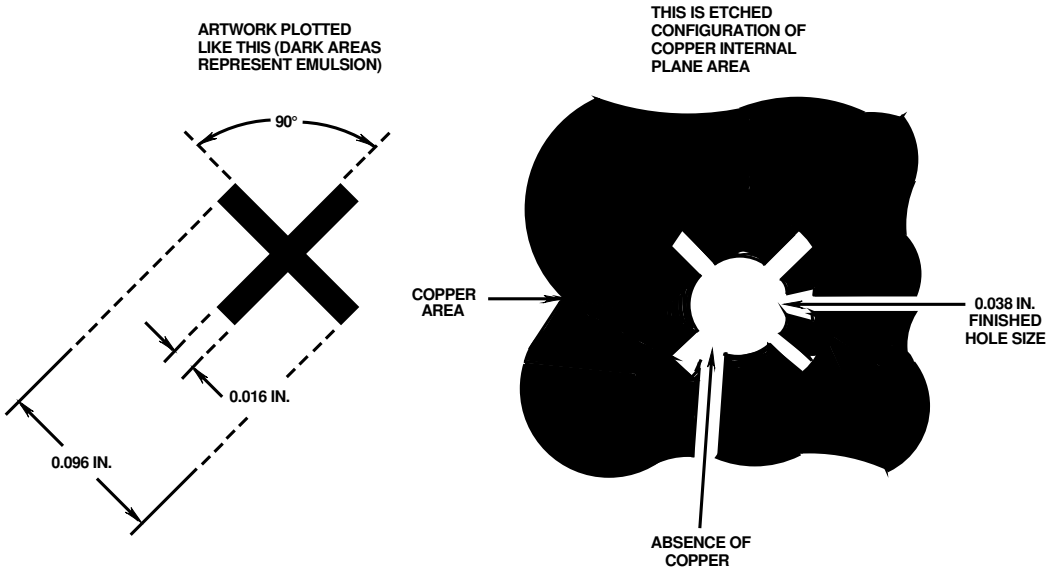
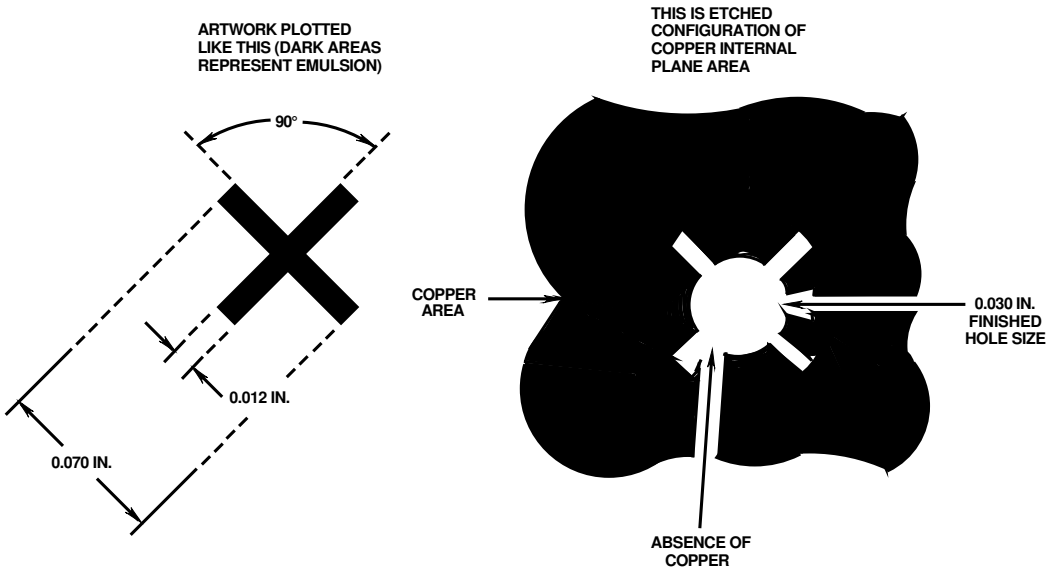

ARTWORK PLOTTED LIKE THIS (DARK AREAS REPRESENT EMULSION)
90°
0.016 IN.
0.096 IN.
THIS IS ETCHED CONFIGURATION OF COPPER INTERNAL PLANE AREA
COPPER AREA
0.038 IN. FINISHED HOLE SIZE
ABSENCE OF COPPER

Exhibit 18B: Recommended for 0.100–Inch Grid and Finished Hold Size ≥ 0.030 Inch ≤ 0.055 Inch for Improved Signal Integrity


ARTWORK PLOTTED LIKE THIS (DARK AREAS REPRESENT EMULSION)
90°
0.012 IN.
0.070 IN.
THIS IS ETCHED CONFIGURATION OF COPPER INTERNAL PLANE AREA
COPPER AREA
0.030 IN. FINISHED HOLE SIZE
ABSENCE OF COPPER

RULE 4610: THERMAL IMPEDANCE CONNECTIONS FOR LARGE HOLE SIZES

Finished holes larger than 0.055 inch in diameter cannot be used with the standard thermal impedance pad. Components requiring mounting holes larger than 0.055 inch may be connected to the plane as follows.

a. Use alternate connections using vias as shown in Exhibit 19.

b. Create an enlarged version of the VAXBI Thermal Impedance Pad as shown in Exhibit 20.

NOTE

Exhibit 20A shows thermal impedance pad for 0.056 to 0.078 finished hole size.
Exhibit 20B shows thermal impedance pad for 0.079 to 0.093 finished hole size.

Exhibit 19: An Application That Does Not Require a Thermal Impedance Pad

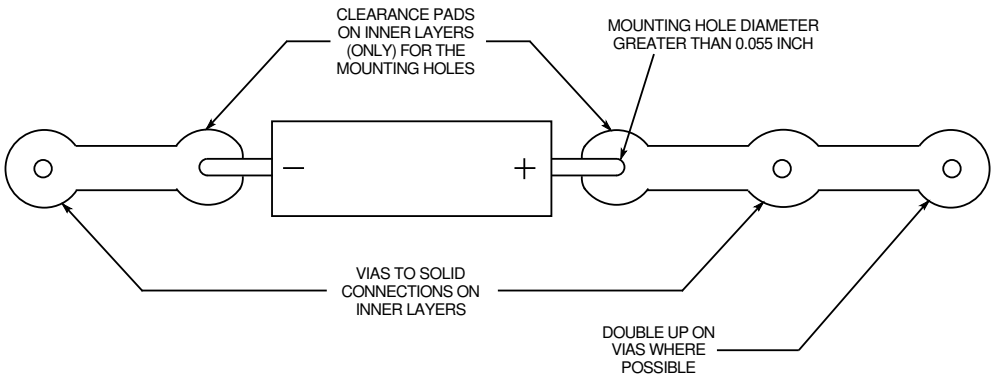

CLEARANCE PADS ON INNER LAYERS (ONLY) FOR THE MOUNTING HOLES
MOUNTING HOLE DIAMETER GREATER THAN 0.055 INCH
VIAS TO SOLID CONNECTIONS ON INNER LAYERS
DOUBLE UP ON VIAS WHERE POSSIBLE

Exhibit 20: Enlarged VAXBI Thermal Impedance Pad for Large Diameter Holes (Note: Drawings not to scale)

Exhibit 20A: Thermal Impedance Pad for 0.056 to 0.078 Finished Hole Size

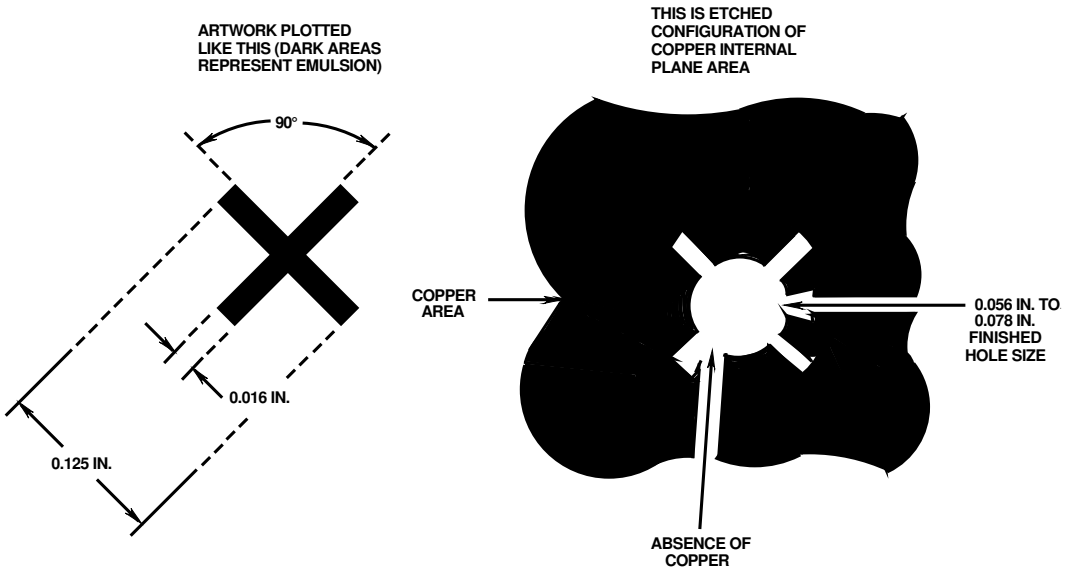
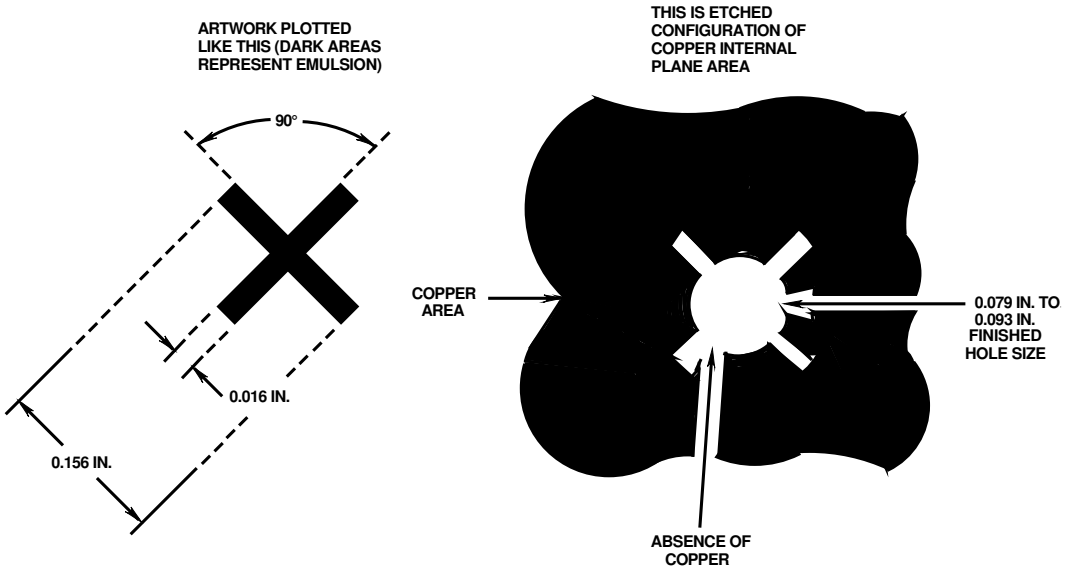

ARTWORK PLOTTED LIKE THIS (DARK AREAS REPRESENT EMULSION)
90°
0.016 IN.
0.125 IN.
THIS IS ETCHED CONFIGURATION OF COPPER INTERNAL PLANE AREA
COPPER AREA
0.056 IN. TO 0.078 IN. FINISHED HOLE SIZE
ABSENCE OF COPPER

Exhibit 20B: Thermal Impedance Pad for 0.079 to 0.093 Finished Hole Size


ARTWORK PLOTTED LIKE THIS (DARK AREAS REPRESENT EMULSION)
90°
0.016 IN.
0.156 IN.
THIS IS ETCHED CONFIGURATION OF COPPER INTERNAL PLANE AREA
COPPER AREA
0.079 IN. TO 0.093 IN. FINISHED HOLE SIZE
ABSENCE OF COPPER

3.9 MULTISIGNAL LAYER REQUIREMENTS

Standard MSL layups are found in EL-ENPCB-02.

Multisignal layer (MSL) PWBs are defined in *DEC STD 016-0 Printed-Wiring Boards and Module Manufacturing Terminology*. MSL PWBs are available in the standard fingerless (FICs) and finger circuits shown in DEC STD 030-1, Exhibit 8 through DEC STD 030-1, Exhibit 14, and are subject to the same basic artwork, component, circuit outline, product safety, standard grid, and testability requirements as ML circuits, except as specifically noted throughout this standard or as indicated in this subhead.

RULE 4650: NONFUNCTIONAL (UNUSED) INNER LAYER PADS

Nonfunctional (unused) inner layer pads shall be supplied in the design data.

RULE 4655: LAYUP SYMMETRY

To minimize warpage, the arrangement of all copper and dielectric layers shall be symmetric with respect to the centerline of the PWB in the Z-Axis. This symmetry requires an even number of copper layers.

RULE 4660: SIGNAL-OVER-PLANE LAYUP CONSTRUCTION

To enhance dimensional stability and enable better control of dielectric thickness, the ML/MSL layup that enables the PWB fabricator to select signal-over-plane inner layer cores shall be considered as the preferred layup.

3.10 PLANAR RESISTOR TECHNOLOGY (PRT)

The following subheads define the design recommendations and rules for planar resistor technology. Exhibit 21 shows the planar resistor configuration. Consult the owner of this section of DEC STD 030 for guidance in the use of PRT.

Refer to heading 3.5.3.3 for PRT bare board test requirements, and Rule 4315 for HIPOT test requirements.

3.10.1 PRT Recommendations

Power dissipation limits must be considered for heat control. The resistor value for this technology is ± 10 percent of the nominal value. Avoid using resistor values below 10 ohms.

Spare planar resistors should be provided for each resistor value used on a layer. This is recommended for ease of ECO and rework.

3.10.2 PRT Rules

RULE 4670: PRT LAYUP

The planar resistor layer shall not be placed on an external layer in the board layup. This is required to protect the resistors against handling damage.

Recommendation: The planar resistor layer should be positioned in the board layup so it is immediately adjacent to an outer layer. This is recommended for ease of ECO.

RULE 4680: COPPER FOIL THICKNESS FOR PRT TECHNOLOGY

Copper foil weight greater than 1 ounce shall not be used for the planar resistor layer. This is required to maintain resistor tolerance control.

Recommendation: When 1-ounce weight copper foil is inadequate for electrical reasons, an additional copper plane should be added to the layup on the other side of the resistive layer core.

RULE 4690: lAMINATE CORE THICKNESS OF PRT LAYER

The laminate core thickness supporting the planar resistor layer shall be 0.0062 inch minimum to prevent damage during lamination.

RULE 4700: sHEET RESISTANCE VALUE OF PRT LAYER

The sheet resistance value of the planar resistor layer shall be 25 ohms per square.

RULE 4710: MINIMUM PLANAR RESISTOR WIDTH

The minimum planar resistor width shall be 0.020 inch. See Exhibit 21.

RULE 4720: MINIMUM PLANAR RESISTOR LENGTH

The minimum length of the resistive element of the planar resistor shall be 0.020 inch. See Exhibit 21.

RULE 4730: LENGTH OF COPPER CONNECTION BETWEEN THE RESISTIVE ELEMENT OF A PLANAR RESISTOR AND A VIA PAD

The length of the copper connection between the resistive element of a planar resistor and a via pad shall be 0.015 inch minimum. This is required for thermal stress relief. See Exhibit 21.

RULE 4740: LENGTH OF COPPER CONNECTION BETWEEN THE RESISTIVE ELEMENT OF A PLANAR RESISTOR AND THE PLANE

The length of the copper connection between the resistive element of a planar resistor and a plane shall be 0.015 inch minimum. This is required for the board manufacturing process. See Exhibit 21.

RULE 4750: WIDTH OF COPPER CONNECTION BETWEEN THE RESISTIVE ELEMENT OF THE PLANAR RESISTOR AND THE PLANE

The width of the copper connection between the resistive element of the planar resistor and the plane shall not be less than the width of any connections in the network to which the resistor is attached. The minimum is 0.015 inch. See Exhibit 21.

CAUTION

Exercise caution when positioning planar resistors adjacent to each other and in different orientations. This is required to prevent current carrying capacity and disconnection from the plane.

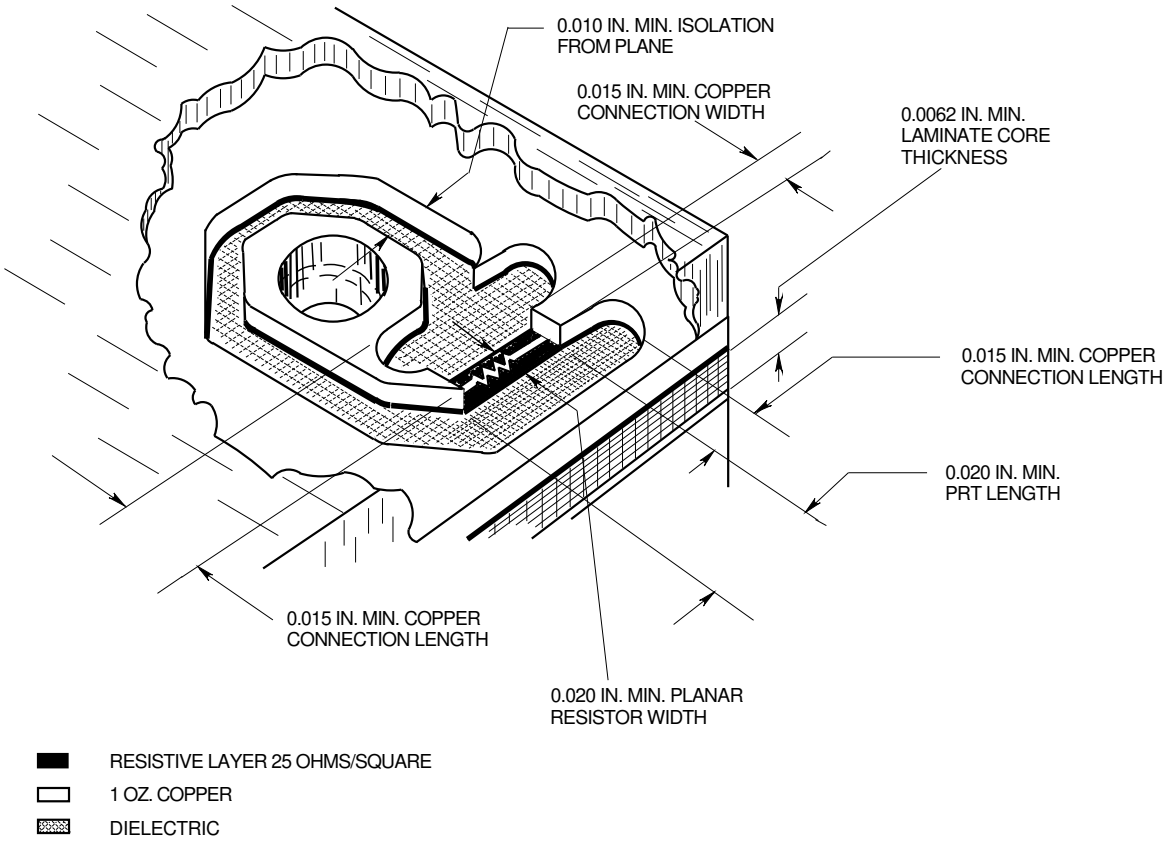
RULE 4760: PLANAR RESISTOR ISOLATION FROM THE PLANE

The resistive element of the planar resistor shall be isolated from the plane by at least 0.010 inch.

RULE 4780: PLANAR RESISTOR SPACING REQUIREMENTS

The resistive element of the planar resistor shall be isolated from other resistors and conductive features by a minimum of 0.010 inch; however, adjacent resistors can share the same 0.010-inch clearance area.

Exhibit 21: Planar Resistor Configuration


0.010 IN. MIN. ISOLATION FROM PLANE
0.015 IN. MIN. COPPER CONNECTION WIDTH
0.0062 IN. MIN. LAMINATE CORE THICKNESS
0.015 IN. MIN. COPPER CONNECTION LENGTH
0.020 IN. MIN. PRT LENGTH
0.015 IN. MIN. COPPER CONNECTION LENGTH
0.020 IN. MIN. PLANAR RESISTOR WIDTH
RESISTIVE LAYER 25 OHMS/SQUARE
1 OZ. COPPER
DIELECTRIC

3.11 CONTROLLED IMPEDANCE DESIGN REQUIREMENTS

This subhead specifies the required design elements for controlled impedance test modules. The line width, copper weight, dielectric thickness, and dielectric type determine the impedance control characteristics of the etched circuit. Power and ground planes function as reference planes for impedance-controlled designs.

Controlled impedance test coupons are used on multilayer circuits in locations that represent average plating, etching, and laminating capabilities. They should be placed within the circuit area where space permits. Exhibit 23 shows the test coupon.

RULE 4800: PROXIMITY OF TRANSMISSION LINES TO REFERENCE PLANE OPENINGS AND EDGES

Transmission lines shall be adequately spaced from the edges of openings in their associated reference plane, such as split planes, void areas, venting stripes, ground plane perimeter, inner layer clearance pads, and others. The actual minimum spacing shall be determined by signal integrity analysis, and conductors shall be routed accordingly.

NOTE

Transmission lines that are spaced inadequately or *run off* their associated reference plane create signal integrity problems that are exceedingly difficult to identify and troubleshoot.

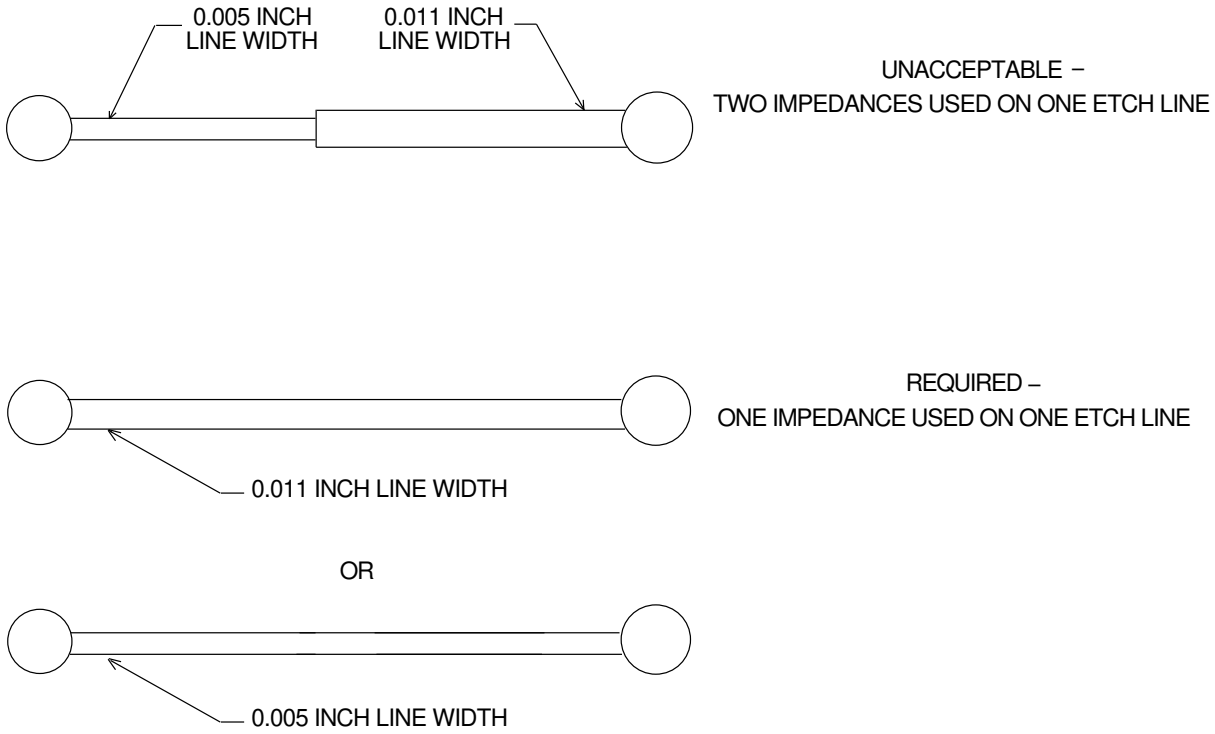
RULE 4900: CONTROLLED IMPEDANCE TESTING - GENERAL

When impedance testing is required, a test coupon shall be supplied and documented per *DEC STD 140-1, Documentation Requirements for Printed-Wiring Boards (50-Class)*. For each impedance value, the line width used in the test coupon shall be the same as that of the actual controlled impedance circuit line width. It is preferred that only one value of controlled impedance line be tested for each controlled impedance layer.

RULE 4905: CONTROLLED IMPEDANCE TESTING - MULTIPLE IMPEDANCE VALUES

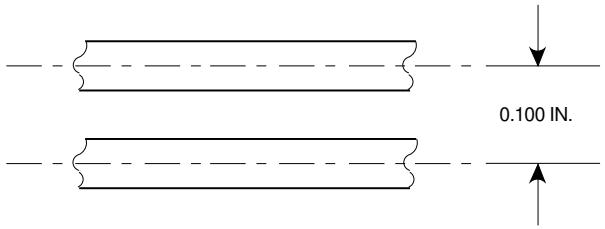
When multiple impedance values must be tested on the same layer, multiple etch lines must be used in the test coupon. Only one controlled impedance value per etch line is allowed. See Exhibit 22.

Exhibit 22: Multiple Impedance Values



RULE 4907: MINIMUM CONTROLLED IMPEDANCE ETCH LINE CENTER-TO-CENTER DISTANCE

When two etch lines are on the same layer of the test coupon, minimum center-to-center distance shall be 0.100 inch.



RULE 4910: CONTROLLED IMPEDANCE SOLDERMASK REQUIREMENTS

When soldermask is used, the coupon and the board shall have the same soldermask requirements with respect to the transmission lines.

RULE 4915: CONTROLLED IMPEDANCE TEST COUPON CLEARANCE REQUIREMENTS

There shall be no conductive material within 0.100 inch of the test coupon with the exception of power and ground planes. (This is a via restrict zone.) See Exhibit 23.

RULE 4920: CONTROLLED IMPEDANCE COUPON REFERENCE PLANES (POWER/GROUND)

Reference planes shall be continuous without breaks, voids, splits, or interruptions of the foil in the test coupon area.

WARNING

When the reference planes are connected to each other within the test coupon area, the entire coupon shall be isolated from the rest of the circuit area.

RULE 4925: CONTROLLED IMPEDANCE COUPON NOMENCLATURE REQUIREMENTS

Each layer with controlled impedance etch lines shall be identified on side 1 near the PTH at each end of the etch line. Conductive nomenclature (etch) shall be no closer than 0.100 inch to all etch in the coupon area; nonconductive screened nomenclature is allowed within the coupon area. See Exhibit 23.

RULE 4930: CONTROLLED IMPEDANCE TEST COUPON REFERENCE PLANE DESIGNATION

Square pads shall be used in the test coupon to designate the reference planes. See Exhibit 23.

RULE 4935: CONTROLLED IMPEDANCE–TEST COUPONS OUTSIDE THE FINISHED CIRCUIT AREA

Controlled impedance test coupons that cannot be designed within the finished circuit area must be designed as separate circuits to be positioned by the PWB fabricator, unless otherwise specified by the design engineer. Refer to DEC STD 176-0 for further information on positioning requirements.

Controlled impedance test coupons that cannot be designed within the finished circuit area shall provide sufficient space (on side 1 or 2) for a vendor code, date code, serial number, and part number.

RULE 4940: CONTROLLED IMPEDANCE–BENDS IN ETCH LINES

Controlled impedance etch lines in the test coupon shall be straight except within 0.500 inch of the test point area where bends may be required. See Exhibit 23.

RULE 4945: CONTROLLED IMPEDANCE - USE OF THERMAL RELIEF PADS WITHIN THE TEST COUPON AREA

Thermal relief pads shall not be used within the test coupon area.

RULE 4950: CONTROLLED IMPEDANCE–SIMULATION OF CROSSOVER CAPACITANCE

When etch on adjacent layers in the actual PWB design is routed orthogonally, a pattern shall be added to the coupon that simulates the *crossover* capacitance. The pattern line width shall be the same as the design line width and crossovers shall be placed at four times the routing grid. The clearance from the controlled impedance line to the pattern shall be 0.010 inch, and the pattern line length shall be 0.080 inch. See Exhibit 25.

RULE 4955: CONTROLLED IMPEDANCE–MINIMUM ETCH LINE LENGTHS

Controlled impedance etch line within the test coupon shall be a minimum of 6.0 inches long from hole center to hole center. All controlled impedance etch lines within the coupon should be of equal length. Where measurement of propagation delay is required, all transmission lines shall be of equal length. See Exhibit 23.

RULE 4960: CONTROLLED IMPEDANCE–TEST PROBE PATTERNS

Typical test coupon probe patterns, for various SMA probes, are shown in Exhibit 24. The following hole/pad sizes should be used.

	Single Impedance (Patterns 1A & 1B)	Single Impedance (Pattern 2)	Dual Impedance (Pattern 3)
Signal Pad Diameter (Inch)	0.080	0.060	0.060
P/G Pad (Square)	0.080	0.060	0.060
Clearance Pad Diameter	0.100	0.080	0.080
Finished Hole Size Diameter	0.062	0.038	0.038

Exhibit 23: Suggested Dual Impedance Test Coupon Area

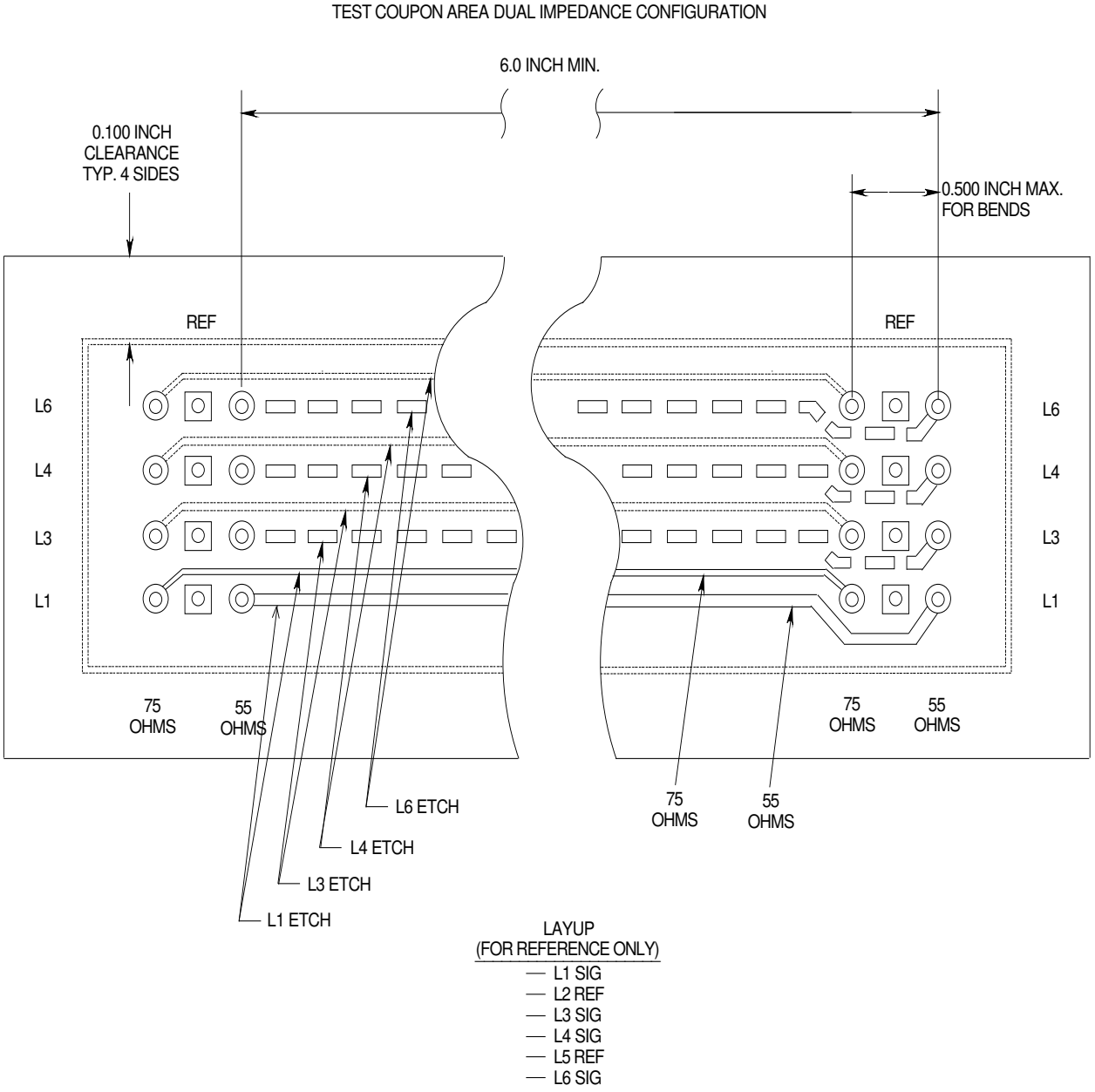
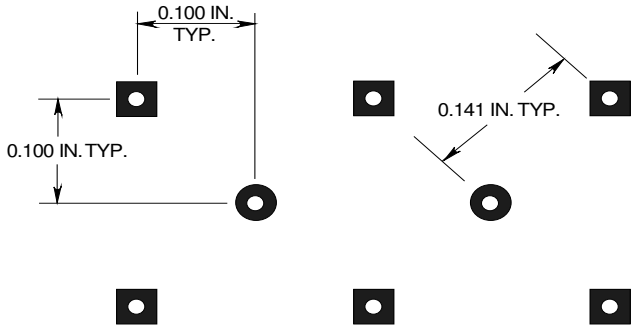


Exhibit 24: Required Test Coupon Probe Patterns

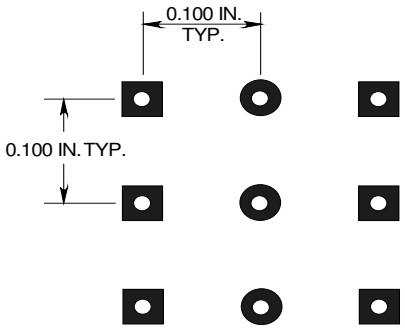
SINGLE IMPEDANCE TEST COUPON
PROBE PATTERN 1A



0.080 In. Signal Pad Diameter
0.080 In. P/G Pad (Square)
0.100 In. Clearance Pad Diameter
0.062 In. Finished Hole Diameter

Standard SMA Probe (5–Pin)

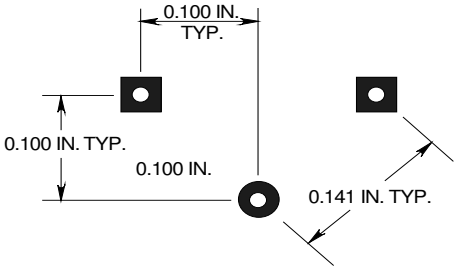
SINGLE IMPEDANCE TEST COUPON
PROBE PATTERN 2



0.060 In. Signal Pad Diameter
0.060 In. P/G Pad (Square)
0.080 In. Clearance Pad Diameter
0.038 In. Finished Hole Diameter

0.100–Inch 2–Pin SMA Probe (Custom)

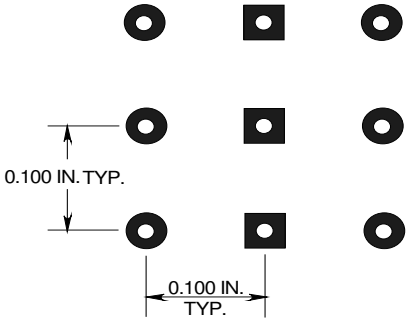
SINGLE IMPEDANCE TEST COUPON
PROBE PATTERN 1B



0.080 In. Signal Pad Diameter
0.080 In. P/G Pad (Square)
0.100 In. Clearance Pad Diameter
0.062 In. Finished Hole Diameter

Modified SMA Probe (2 or 3 Pin)

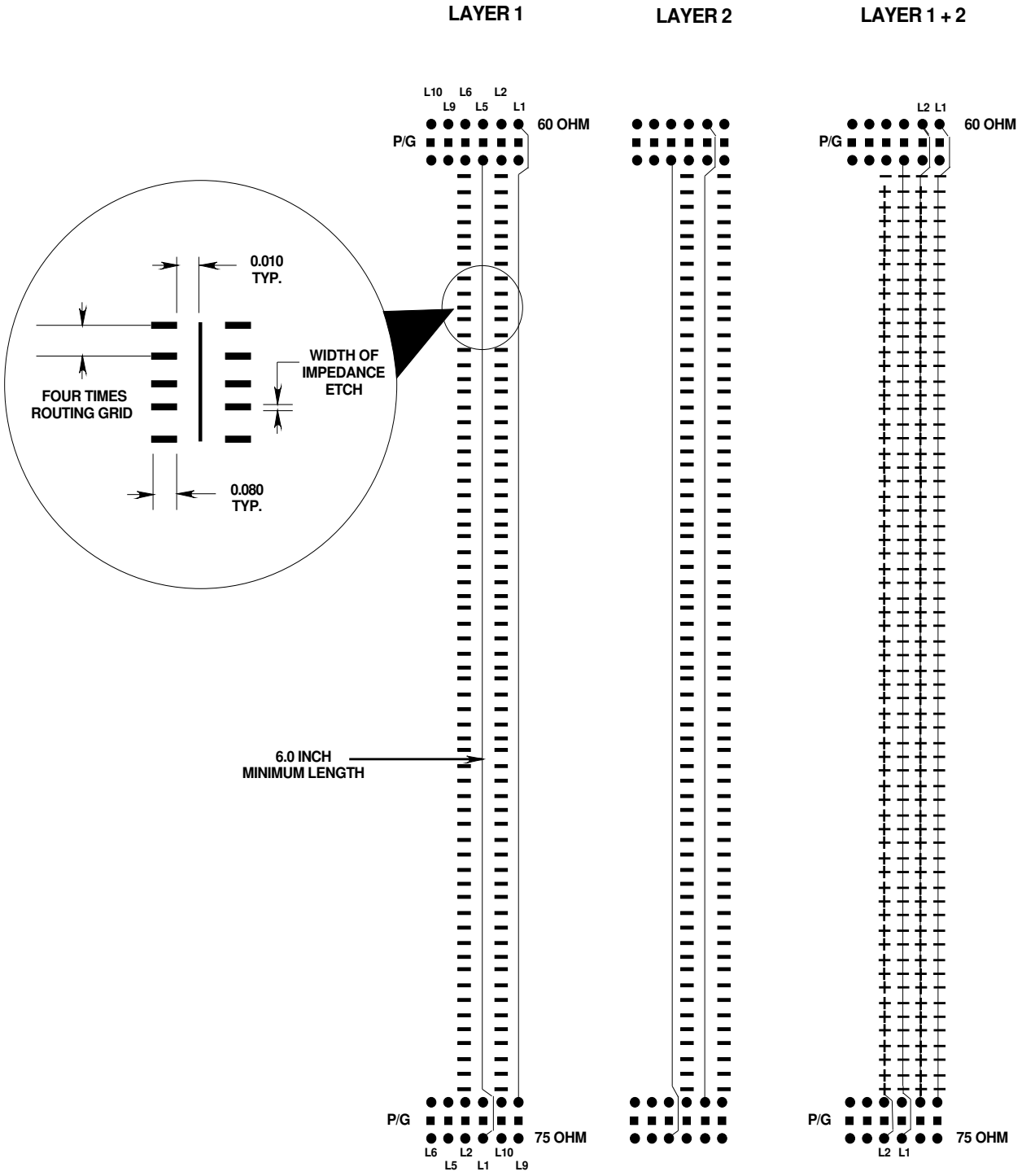
DUAL IMPEDANCE TEST COUPON
PROBE PATTERN 3



0.060 In. Signal Pad Diameter
0.060 In. P/G Pad (Square)
0.080 In. Clearance Pad Diameter
0.038 In. Finished Hole Diameter

0.100–Inch 2–Pin SMA Probe (Custom)

Exhibit 25: Cross Hatching for Orthogonal Routing



APPENDIX A - STANDARD CIRCUIT TECHNOLOGY

This appendix includes standard circuit technology definitions (Exhibit 26), associated inner layer clearance pad tables (Exhibit 27), and minimum spacing reference tables (Exhibit 28). The definitions given in Exhibit 26 are based on Gerber Photoplotter Aperture Wheel restrictions and are no longer valid for defining manufacturability limits. They have, however, been used for past designs, and designs meeting these requirements are still highly manufacturable. For this reason, these three exhibits have been retained for reference purposes.

NOTE

Do not use standard technology definition titles, such as HD1, HD2, and FL1, in future product documentation. Refer to *DEC STD 140-1 Documentation Requirements for Printed-Wiring Boards (50-Class)*.

Exhibit 26: Technology Definitions

STANDARD DENSITY (SD) (Sheet 1 of 8)
DEC STD 030 GDC CODE (BLOCK 1): B

Finished PWB Features (inches)

Basic Definition: 0.020–inch nominal line widths
0.020–inch nominal conductor–to–conductor spacing

PAD SIZES		DEFINED HOLE SIZES
1.	0.080	**UNPLATED**
2.	0.085	
3.	0.100	0.038 through 0.124
4.	0.125	0.125 through 0.250
5.	0.187	0.157 (tooling)
6.	0.080 square	0.250 (tooling)
7.	Heat Relief – Inner/Outer Diameter 0.070 X 0.100	0.251 and over
LINE SIZES		**PLATED**
		Component
8.	0.020	0.032
9.[2]	0.025	0.038
10.	0.030	0.041 (Press–Pin)
11.	0.037	0.042
12.	0.042	
13.	0.043	**Via**
14.[2]	0.050	
15.	0.085	0.038
16.[2]	0.100	
17.[2]	Undisclosed	**Other**
		0.063 and under
		0.064 through 0.124
		0.125 through 0.250
		0.251 and over

Note 1. A total of 17 pads/lines may be used from the above selection.
Note 2. Four positions are predefined, one of which is undisclosed.

HIGH DENSITY #1 (HD1) (Sheet 2 of 8)
DEC STD 030 GDC CODE (BLOCK 1): C

Finished PWB Features (inches)

Basic Definition: 0.015–inch nominal line widths
0.015–inch nominal conductor–to–conductor spacing

PAD SIZES		DEFINED HOLE SIZES
1.	0.055	**UNPLATED**
2.	0.060	
3.	0.065	0.038 through 0.250
4.	0.075	0.125 through 0.250
5.	0.080	0.157 (tooling)
6.	0.085	0.250 (tooling)
7.	0.100	0.251 and over
8.	0.125	
9.	0.187	
10.	Heat Relief – Inner/Outer Diameter 0.070 X 0.100	**PLATED**
11.	0.040 (pad expansion only)	**Component**
12.	0.080 square	0.032 0.038 0.041 (Press–Pin) 0.042
LINE SIZES		**Via**
13.	0.015	0.038
14.	0.020	
15.[2]	0.025	**Other**
16.	0.030	
17.	0.037	0.032 through 0.063
18.	0.042	0.064 through 0.124
19.	0.043	0.125 through 0.250
20.[2]	0.050	0.251 and over
21.	0.085	
22.[2]	0.100	
23.[2]	Undisclosed	

Note 1. A total of 23 pads/lines may be used from the above selection.
Note 2. Four positions are predefined, one of which is undisclosed.

HIGH DENSITY #2 (HD2) (Sheet 3 of 8)
DEC STD 030 GDC CODE (BLOCK 1): D

Finished PWB Features (inches)

Basic Definition: 0.012–inch nominal line widths
0.013–inch nominal conductor–to–conductor spacing

PAD SIZES		DEFINED HOLE SIZES
1.	0.055	**UNPLATED**
2.	0.060	
3.	0.065	0.038 through 0.250
4.	0.075	0.125 through 0.250
5.	0.080	0.157 (tooling)
6.	0.085	0.250 (tooling)
7.	0.100	0.251 and over
8.	0.125	
9.	0.187	
10.	Heat Relief – Inner/Outer Diameter 0.070 X 0.100	**PLATED**
11.	0.040 (pad expansion only)	**Component**
12.	0.080 square	0.032 0.038 0.041 (Press–Pin) 0.042
LINE SIZES		**Via**
13.	0.012	0.038
14.	0.015	
15.	0.020	**Other**
16.[2]	0.025	
17.	0.030	0.032 through 0.063
18.	0.037	0.064 through 0.124
19.	0.042	0.125 through 0.250
20.	0.043	0.251 and over
21.[2]	0.050	
22.	0.085	
23.[2]	0.100	
24.[2]	Undisclosed	

Note 1. A total of 24 pads/lines may be used from the above selection.
Note 2. Four positions are predefined, one of which is undisclosed.

(Sheet 4 of 8)

FINE LINE #1 (FL1)
DEC STD 030 GDC CODE (BLOCK 1): E

Finished PWB Features (inches)

Basic Definition: 0.008–inch nominal line widths
0.008–inch nominal conductor–to–conductor spacing

PAD SIZES		DEFINED HOLE SIZES
1.	0.040	**UNPLATED**
2.	0.055	
3.	0.060	0.038 through 0.124
4.	0.075	0.125 through 0.250
5.	0.080	0.157 (tooling)
6.	0.085	0.250 (tooling)
7.	0.100	0.251 and over
8.	0.125	
9.	0.187	
10.	Heat Relief – Inner/Outer Diameter 0.070 X 0.100	**PLATED**
11.	0.055 square	**Component**
12.	0.080 square	0.032 0.038 0.041 (Press–Pin) 0.042
LINE SIZES		**Via**
13.	0.008	0.038
14.	0.012	
15.	0.015	**Other**
16.	0.020	
17.[2]	0.025	0.032 through 0.063
18.	0.030	0.064 through 0.124
19.	0.037	0.125 through 0.250
20.[2]	0.050	0.251 and over
21.	0.070	
22.	0.085	
23.[2]	0.100	
24.[2]	Undisclosed	

Note 1. A total of 24 pads/lines may be used from the above selection.
Note 2. Four positions are predefined, one of which is undisclosed.

FINE LINE #2 (FL2) (Sheet 5 of 8)
DEC STD 030 GDC CODE (BLOCK 1): F

Finished PWB Features (inches)

Basic Definition: 0.006–inch nominal line widths
0.010–inch nominal conductor–to–conductor spacing

PAD SIZES		DEFINED HOLE SIZES
1.	0.040	**UNPLATED**
2.	0.060	
3.	0.070	0.038 through 0.124
4.	0.080	0.125 through 0.250
5.	0.085	0.157 (tooling)
6.	0.100	0.250 (tooling)
7.	0.125	0.251 and over
8.	0.187	
9.	Heat Relief – Inner/Outer Diameter 0.070 X 0.100	**PLATED**
		Component
10.	0.060 square	0.032
11.	0.080 square	0.038
LINE SIZES		0.041 (Press–Pin)
		0.042
12.	0.006	**Via**
13.	0.008	
14.	0.010	0.038
15.	0.012	
16.	0.015	**Other**
17.	0.018	
18.[2]	0.025	0.032 through 0.063
19.[2]	0.050	0.064 through 0.124
20.[2]	0.100	0.125 through 0.250
21.[2]	Undisclosed	0.251 and over
22.[2]	Undisclosed	
23.[2]	Undisclosed	
24.[2]	Undisclosed	

Note 1. A total of 24 pads/lines may be used from the above selection.
Note 2. Seven positions are predefined, four of which are undisclosed.

(Sheet 6 of 8)

FINE LINE #3 – MSL: VAXBI AND SMT (FL3)
DEC STD 030 GDC CODE (BLOCK 1): F

Finished PWB Features (inches)

Basic Definition: 0.006–inch nominal line widths
0.010–inch nominal conductor–to–conductor spacing

PAD SIZES		DEFINED HOLE SIZES
1.	0.040	**UNPLATED**
2.	0.060	
3.	0.070	0.038 through 0.124
4.	0.080	0.125 through 0.250
5.	0.100	0.157 (tooling)
6.	0.125	0.250 (tooling)
7.	0.187	
8.	X–Shaped Heat Relief – Inner/Outer Diameter 0.016 X 0.096	
9.	0.060 square	**PLATED**
10.	0.080 square	**Component**
11.	Heat Relief – Inner/Outer Diameter 0.070 X 0.100	0.032 0.038 0.041 (Press–Pin) 0.042
LINE SIZES		**Via**
12.	0.006	0.038
13.	0.008	
14.	0.010	**Other**
15.	0.012	
16.	0.015	0.032 through 0.063
17.	0.018	0.064 through 0.124
18.[2]	0.025	0.125 through 0.250
19.	0.030	0.251 and over
20.	0.040	
21.[2]	0.050	
22.	0.060	
23.[2]	0.100	
24.[2]	Undisclosed	

Note 1. A total of 24 pads/lines may be used from the above selection.
Note 2. Four positions are predefined, one of which is undisclosed.

(Sheet 7 of 8)

FINE LINE #4 – PREFERRED SMT TECHNOLOGY DEFINITION (FL4)
DEC STD 030 GDC CODE (BLOCK 1): F

Finished PWB Features (inches)

Basic Definition: 0.005–inch nominal line widths
0.005–inch nominal conductor–to–conductor spacing

PAD SIZES		TYPICAL USAGE
1.	0.015	Pad expansion for 0.020–0.029 pad
2.	0.025	Via pad/Pad expansion for 0.030–0.044 pad
3.	0.035	Test pad
4.	0.040	Via pad, pad expansion for pads ≥ 0.040, IL, fiducial, test pad
5.	0.060	Standard intrusives, IL clearance
6.	0.080	Standard IL clearance, miscellaneous components
7.	0.125	IL clearance, miscellaneous components
8.	0.187	IL clearance, miscellaneous components
9.	0.040 X 0.025 Donut	Laminated–blind vias (must be used for IL clearance pad for 0.010 hole)
10.	0.080 X 0.080 Square	Autothieving
11.	0.070 X 0.100 Heat Relief	Standard heat relief
12.	0.016 X 0.096 Heat Relief	X–Shaped heat relief
LINE SIZES		**TYPICAL USAGE**
13.	0.005	Standard line – No volume capability at this time
14.	0.006	Standard line
15.	0.008	Standard line (dispersion)
16.	0.010	Standard line (text)
17.	0.016	Footprint (0.0025 pitch device)
18.	0.025	Footprint (0.050 pitch device) IL splits
19.	0.030	Footprint
20.	0.040	Footprint
21.	0.050	Footprint, fill area
22.	0.060	Footprint
23.	0.080	Footprint
24.	0.100	Fill area

(Sheet 8 of 8)

FINE LINE #4 – PREFERRED SMT TECHNOLOGY DEFINITION (FL4) (Cont.)
DEC STD 030 GDC CODE (BLOCK 1): F

Finished PWB Features (inches)

Basic Definition: 0.005–inch nominal line widths
0.005–inch nominal conductor–to–conductor spacing

PLATED	UNPLATED
Component	0.038 through 0.124
	0.125 through 0.250
0.032	0.157 (tooling)
0.038	0.250 (tooling)
0.041 (Press–Pin)	0.251 and over
0.042	
VIA	**TYPICAL USAGE**
0.010	Laminated–blind vias only (no volume capability at this time)
0.020	Higher level SMT releases
0.038	Preferred via size for all designs
Other	
0.032 through 0.063	
0.064 through 0.124	
0.125 through 0.250	
0.251 and over	

On inner layers, use the clearances listed in Exhibit 27 for various hole sizes and features. Clearances should be consistent in size on all inner layers for any given hole.

Exhibit 27: Preferred Clearances for Negative-Plotted Inner Layers

Finished Hole Diameter (Inches)	Plotted Clearance Pads Diameter (Inches)		
	Minimum Acceptable	Preferred Optimum	Maximum
0.010	0.035	0.040	0.045
0.020	0.045	0.060	0.085
0.021 – 0.040	0.070	0.080	–
0.041 – 0.060	0.080[1]	0.100	–
0.061 – 0.085	0.125	0.156	–
0.086 – 0.116	0.156	0.187	–
0.117 – 0.147	0.187	0.200	–
Larger than 0.147	Min. 0.045 larger than finished hole size	0.100 larger than finished hole size	0.0625 square inch area[2]
OTHER FEATURES:			
Between Conductors	0.020	0.050	–
Between Co–Planar Voltage and Ground Planes[3]	0.020	0.050	0.0625 square inch area[2]
0.157 Through Holes	0.200	0.200	–

Note 1. For press-pin backplanes with 0.041-inch holes, refer to DEC STD 030-7, Rule 7050.
Note 2. Equivalent to 0.250 by 0.250 inch.
Note 3. Ground and power planes may have bus separations for isolation or isolated lines within the plane.

Exhibit 28: PWB Spacing Reference Guide (Minimum Design Parameters)

Technology Line/Space	Conductor–to–Conductor (nominal inch)	Conductor–to–Pad (nominal inch)	Pad–to–Pad (nominal inch)
P/G Plane	N/A	N/A	N/A
20/20	0.020	0.020	0.020
15/15 (8 1/3–Mil Routing Grid)	0.018	0.015	0.015
12/13 (12 ½–Mil Routing Grid)	0.013	0.0165	0.015
8/8 (8 1/3–Mil Routing Grid)	0.0086	0.0098 [1]	0.015
6/10 (8 1/3–Mil Routing Grid)	0.0106	0.0083	0.015
6/6 (6 1/4–Mil Routing Grid)	0.0065	0.0080	0.015
5/5 (5.0–Mil Routing Grid)	0.005	0.005	0.010 [2]

Note 1. If using 0.060-inch pads with 8/8 technology, conductor-to-pad spacing can be 0.0073 inch.
Note 2. Via-to-via spacing when tented. Refer to Rule 4340, DEC STD 030-5, Rule 5147, and DEC STD 030-5, Rule 5610.

REFERENCED DOCUMENTS

EL-Class Digital Documents

EL-Class Number	Document Title
EL-00012-00	*DEC STD 012-0 Part Identification Standard*
EL-00016-00	*DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology*
EL-00030-01	*DEC STD 030-1 Module Manufacturing Standard - General Producibility Requirements*
EL-00030-02	*DEC STD 030-2 Module Manufacturing Standard - Product Safety Requirements*
EL-00030-05	*DEC STD 030-5 Module Manufacturing Standard - Module Assembly and Component Insertion Rules*
EL-00030-06	*DEC STD 030-6 Module Manufacturing Standard - Bare Board and Module Testability Rules*
EL-00030-07	*DEC STD 030-7 Module Manufacturing Standard - Backplane Rules and Related Factors*
EL-00030-10	*DEC STD 030-10 Module Manufacturing Standard - Footprint Patterns for Surface Mount Technology*
EL-00056-00	*DEC STD 056-0 Symbology - Circuit Schematic Requirements*
EL-00056-03	*DEC STD 056-3 Symbology - Discrete Electronic and Electromechanical Component Symbols*
EL-00140-01	*DEC STD 140-1 Documentation Requirements for Printed-Wiring Boards (50-Class)*
EL-00176-00	*DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*
EL-EN057-00	*VAXBI Module Layout Guide*
EL-EN705-00	*Footprint Patterns for Surface Mount Technology*
EL-ENPCB-01	*PC Board Engineering Handbook—Standard Circuit and Finger Detail Drawings*
EL-ENPCB-02	*PC Board Engineering Handbook—Layer Construction Drawings*
EL-ENPCD-TM	*Electrical Design Guide for Printed Circuits*
EL-SM116-01	*Workmanship Standards - Volume 1*
EL-SM119-01	*Corporate Product Safety and Regulations - Volume 1 Information Processing and Business Equipment*

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